Dual N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Surface-mounted package
- ☑ Low gate charge

1.2 Applications

- ☑ Motor driver appliances
- ☑ Adapter appliances
- ☑ High power inverter system

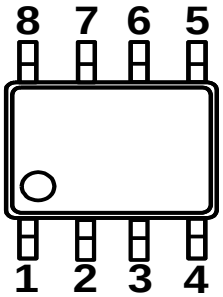
1.3 Quick reference

- ☑ BV ≧ 40 V
- ☑ P_{tot} ≦ 2 W
- ☑ I_D ≦ 11 A
- ☑ $R_{DS(ON)}$ ≦ 10 mΩ @ V_{GS} = 10 V
- ☑ $R_{DS(ON)}$ ≦ 15 mΩ @ V_{GS} = 4.5 V

2. Pin Description

Pin	Description
1	Source(S1)
2	Gate(G1)
3	Source(S2)
4	Gate(G2)
5,6	Drain(D2)
7,8	Drain(D1)

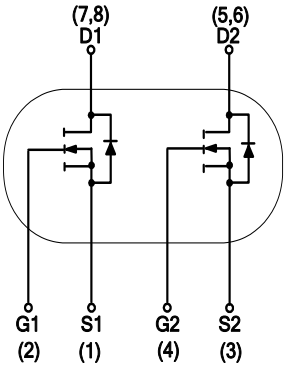
Simplified Outline



Top View

SOP- 8L

Symbol



3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_A = 25 ℃	40	-	V
V_{GS}	Gate-Source Voltage	T_A = 25 ℃	-	± 20	V
I_D*	Drain Current	T_A = 25 ℃, V_{GS} = 10 V	-	11	A
I_{DM}*	Pulsed Drain Current	T_A = 25 ℃, V_{GS} = 10 V	-	44	A
P_{tot}*	Total Power Dissipation	T_A = 25 ℃	-	2	W
T_{stg}	Storage Temperature		- 55	150	℃
T_J	Junction Temperature		-	150	℃
$R_{\theta JC}$*	Thermal Resistance- Junction to Case		-	3.5	℃ / W
$R_{\theta JA}$*	Thermal Resistance- Junction to Ambient		-	62.5	℃ / W

Notes：

* Surface Mounted on 1 in^2 pad area, t ≤ 10 sec

** Pulse width ≤ 10 μs, duty cycle ≤ 1 %

*** Limited by bonding wire

4. Marking Information

Product Name	Marking
KJ4020S	**4020** **YWWXXX** **YWWXXX: Date Code**

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ4020S	**SOP8**			**3000**	

Note: KUAIJIEXIN defines " Green " as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	40	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	1.0	-	2.0	V
I_{DSS}	Drain Leakage Current	V_{DS} = 32 V, V_{GS} = 0 V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{GS} = ± 20 V, V_{DS} = 0 V	-	-	± 100	nA
$R_{DS(ON)}$[a]	Channel On-State Resistance	V_{GS} = 10 V, I_D = 10 A	-	8.5	10	mΩ
	Channel On-State Resistance	V_{GS} = 4.5 V, I_D = 5 A	-	12	15	
Diode Characteristics						
V_{SD}[a]	Diode Forward Voltage	I_{SD} = 10 A, V_{GS} = 0 V	-	-	1.3	V
t_{rr}	Reverse Recovery Time	I_{SD} = 10 A, dI_{SD} / dt = 100 A / μs	-	10	-	nS
Q_{rr}	Reverse Recovery Charge		-	4	-	nC
Dynamic Characteristics[b]						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 20 V Frequency = 1 MHz	-	1628	-	pF
C_{oss}	Output Capacitance		-	112	-	
C_{rss}	Reverse Transfer Capacitance		-	87	-	
t_d(on)	Turn-on Delay Time	V_{DS} = 20 V, V_{GEN} = 10 V, R_G = 4.5 Ω, R_L = 2 Ω, I_{DS} = 10 A	-	6.4	-	nS
t_r	Turn-on Rise Time		-	26	-	
t_d(off)	Turn-off Delay Time		-	34	-	
t_f	Turn-off Fall Time		-	25	-	
Gate Charge Characteristics[b]						
Q_g	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 20 V, I_{DS} = 10 A	-	30	-	nC
Q_{gs}	Gate-Source Charge		-	6	-	
Q_{gd}	Gate-Drain Charge		-	4.5	-	

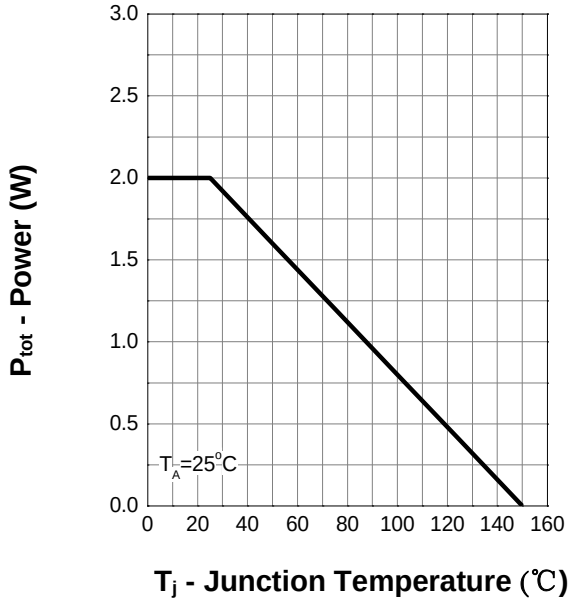
Notes：

a : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2 %

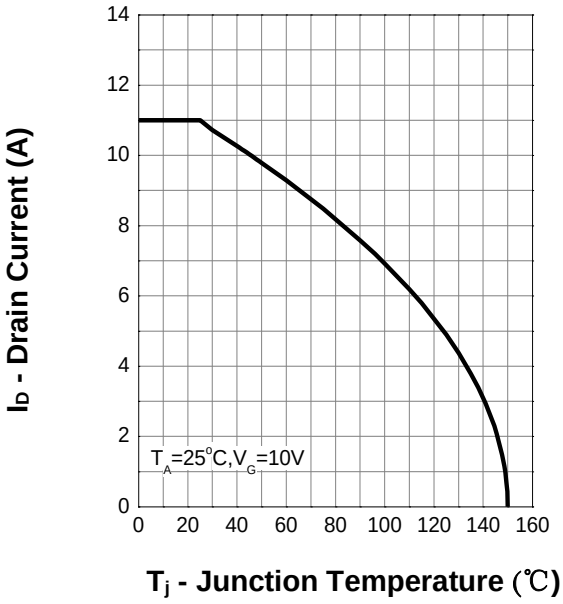
b : Guaranteed by design, not subject to production testing

7. Typical Characteristics

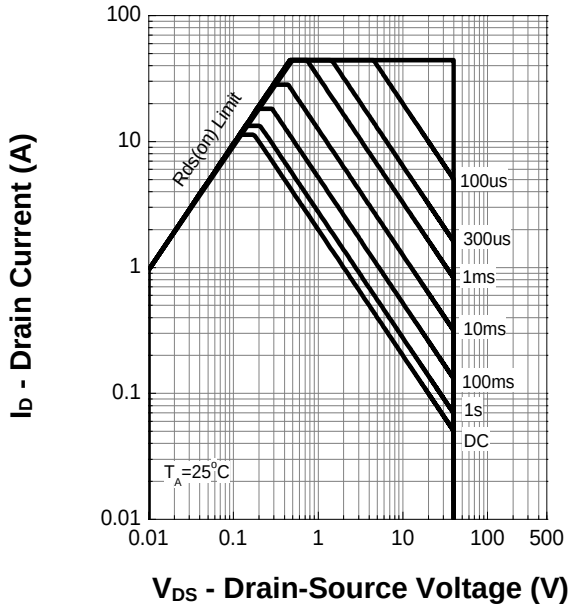
Power Dissipation



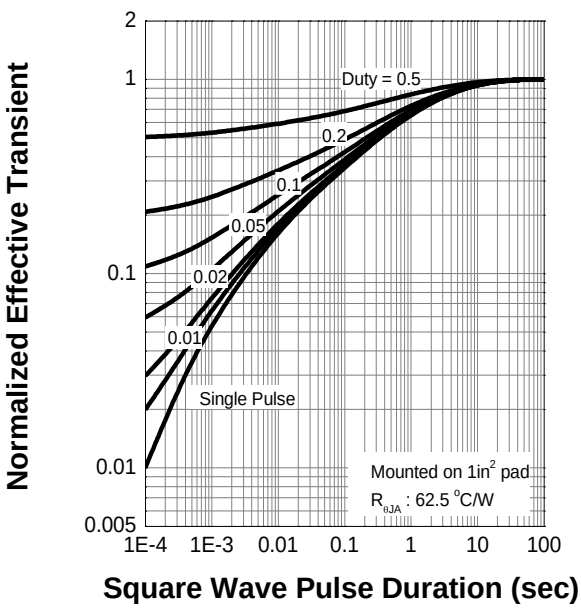
Drain Current



Safe Op、　∩ Area

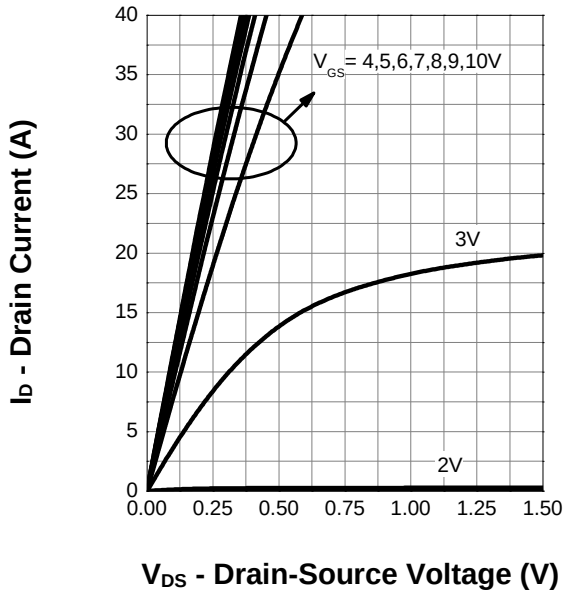


Thermal Transient Impedance

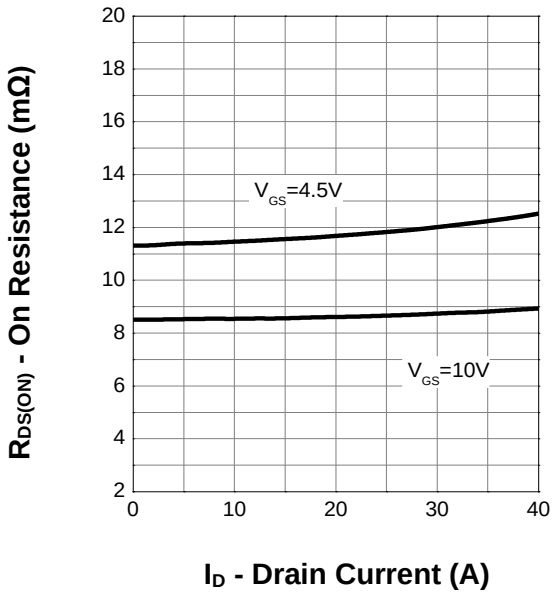


7. Typical Characteristics (cont.)

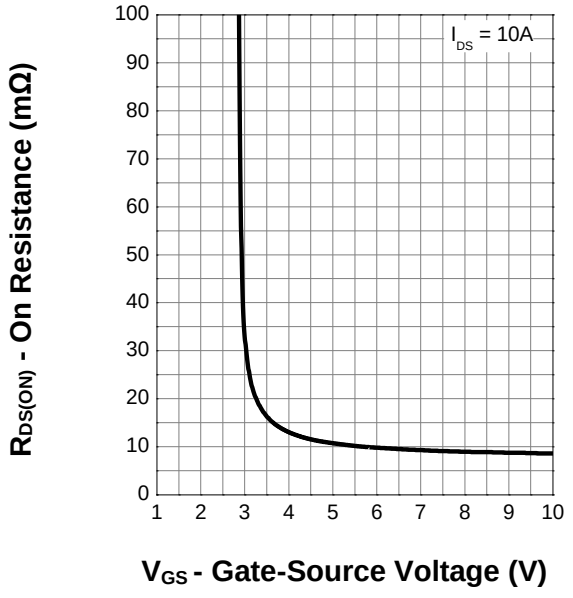
Output Characteristics



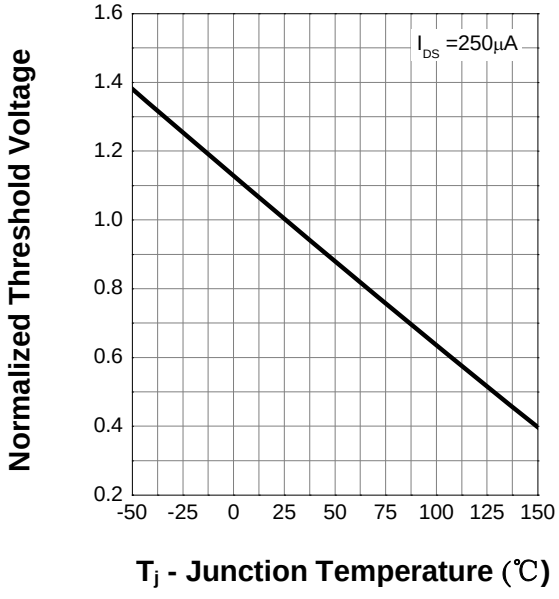
Drain-Source On Resistance



Transfer Characteristics

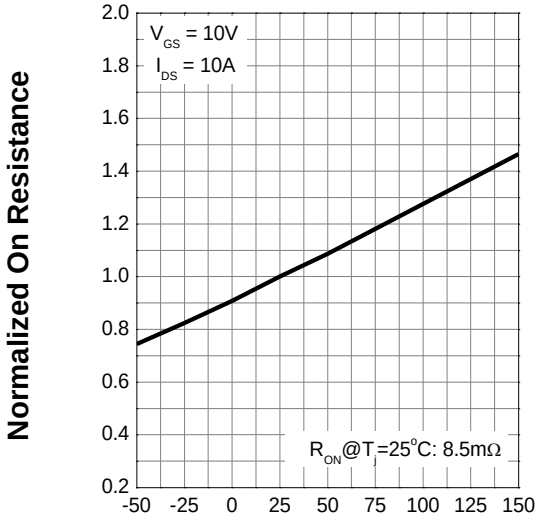


Gate Threshold Voltage

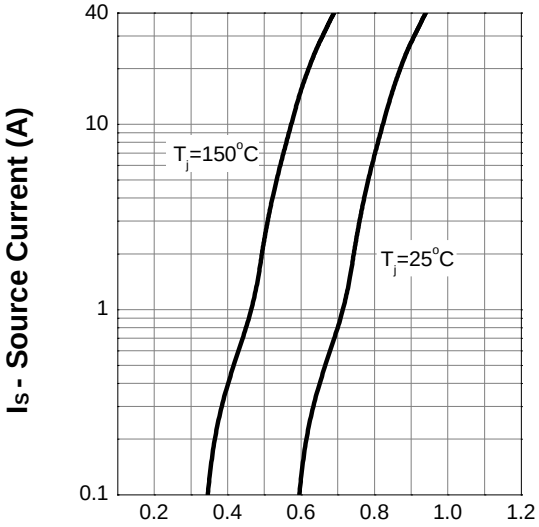


7. Typical Characteristics (cont.)

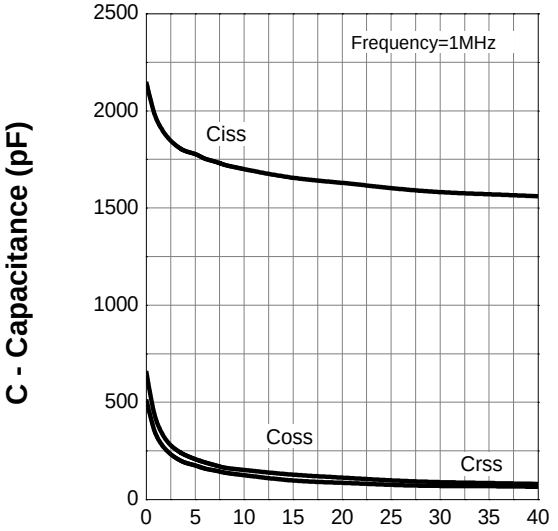
Drain-Source On Resistance



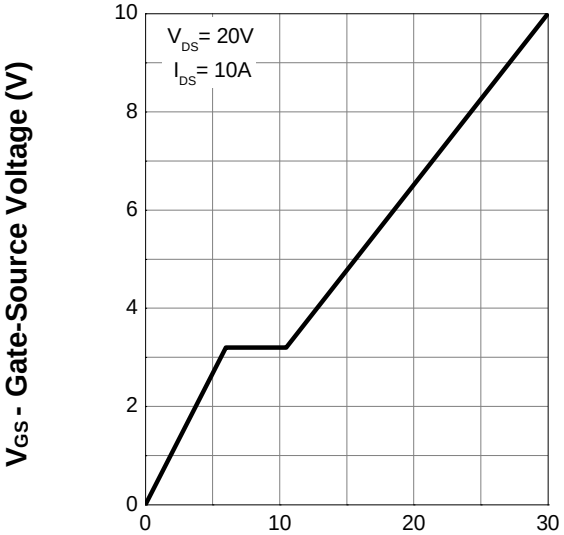
Source-Drain Diode Forward



Capacitance



Gate Charge



8. Package Dimensions

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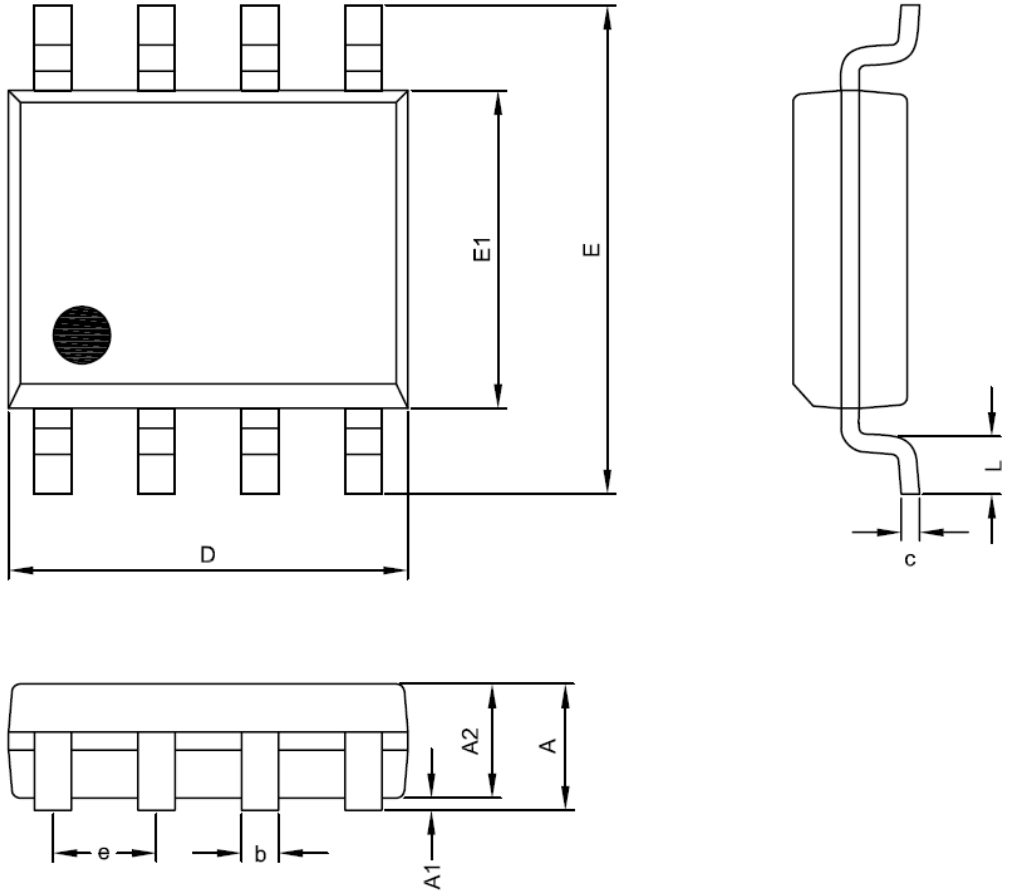

Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes：

1. Jedec outline ： MS-012AA
2. Dimensions ” D ” does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions “ E1 ” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.