

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☒ Surface-mounted package
- ☒ Advanced trench cell design

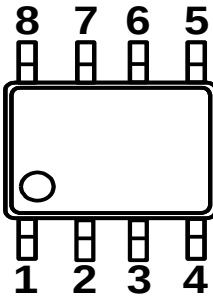
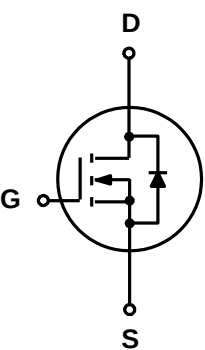
1.2 Applications

- ☒ LCD TV appliances
- ☒ LCDM appliances
- ☒ High power inverter system

1.3 Quick reference

- ☒ $BV \geq 60\text{ V}$
- ☒ $P_{\text{tot}} \leq 2\text{ W}$
- ☒ $I_D \leq 8\text{ A}$
- ☒ $R_{\text{DS(ON)}} \leq 30\text{m}\Omega @ V_{\text{GS}} = 10\text{ V}$
- ☒ $R_{\text{DS(ON)}} \leq 38\text{m}\Omega @ V_{\text{GS}} = 4.5\text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1,2,3	Source(S)	 Top View SOP-8L	
4	Gate(G)		
5,6,7,8	Drain(D)		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	Drain-Source Voltage	T _C = 25 °C	60	-	V
V _{GS}	Gate-Source Voltage	T _C = 25 °C	-	± 20	V
I _D ^{***}	Drain Current (DC)	T _C = 25 °C, V _{GS} = 10 V	-	8	A
		T _C = 100 °C, V _{GS} = 10 V	-	6.4	A
I _{DM} ^{*,***}	Drain Current (Pulsed)	T _C = 25 °C, V _{GS} = 10 V	-	40	A
P _{tot}	Drain power dissipation	T _C = 25 °C	-	2	W
T _{stg}	Storage Temperature		- 55	150	°C
T _J	Junction Temperature		- 55	150	°C
I _S	Continuous-Source Current	T _C = 25 °C	-	8	A
R _{θJA} ^{**}	Thermal Resistance- Junction to Ambient		-	50	°C/W
R _{θJC} ^{**}	Thermal Resistance- Junction to Case		-	62.5	

Notes :

- * Pulse width ≤ 300 μs, duty cycle ≤ 2 %
- ** Mounted on Large Heat Sink
- *** Limited by bonding wire

4. Marking Information

Product Name	Marking
KJ6008S	6008 YWWXXX YWWXXX: Date Code

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ6008S	SOP8			3000	

Note: KUAIJIEXIN defines “ Green ” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics ($T_A=25^\circ$ Unless Otherwise Noted)

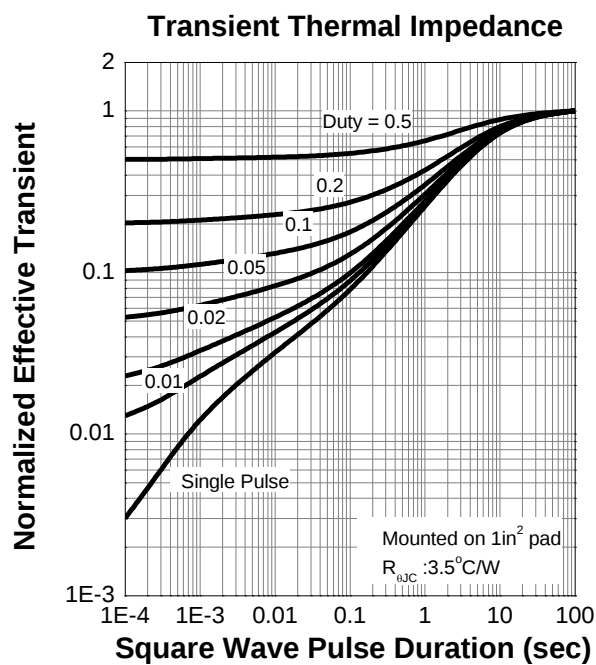
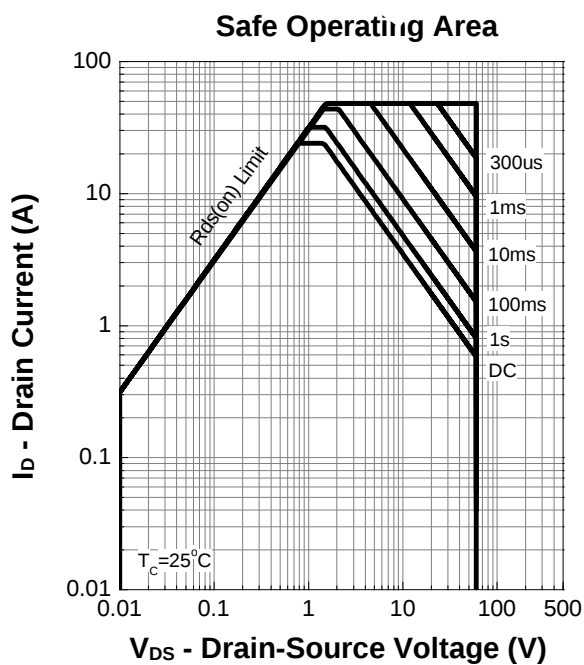
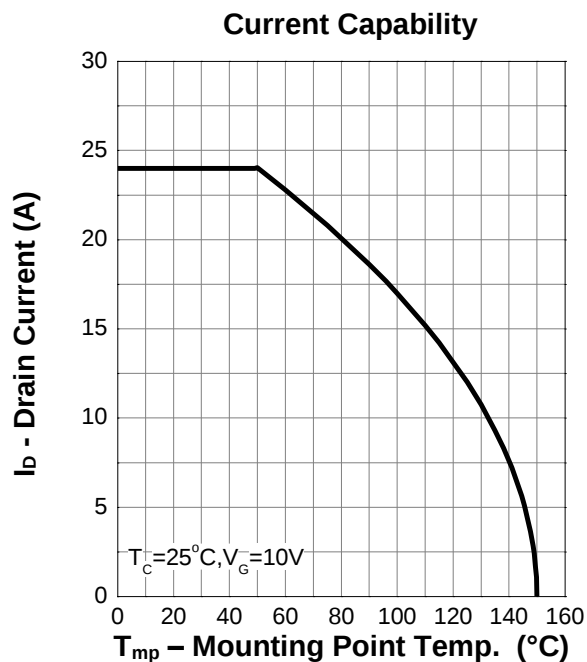
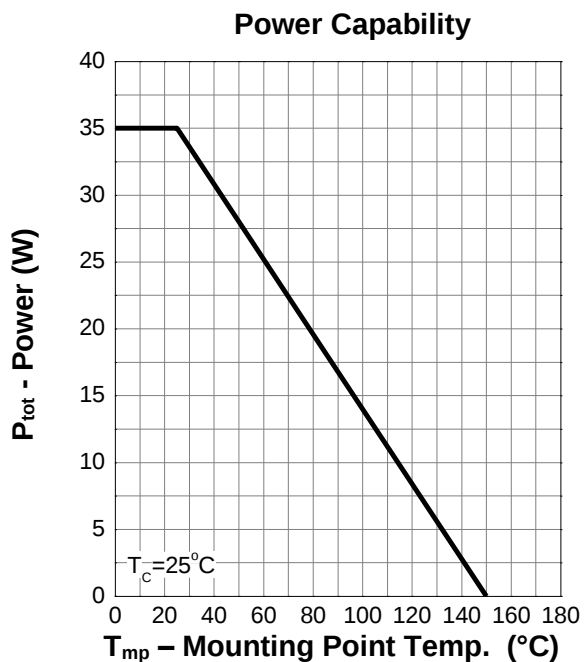
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _{DS} = 250 μA	60	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	1.5	-	2.5	V
I _{DSS}	Drain Leakage Current	V _{DS} = 48 V, V _{GS} = 0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{GS} = 0 V, V _{GS} = ± 20 V	-	-	±100	nA
R _{DS(ON)} ^a	On-State Resistance	V _{GS} = 10 V, I _{DS} = 5 A	-	28	30	m Ω
		V _{GS} = 4.5 V, I _{DS} =3 A	-	33	38	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} = 5 A, V _{GS} = 0 V	-	-	1.3	V
t _{rr}	Reverse Recovery Time	I _{DS} = 5 A, V _{GS} = 0 V dI _{SD} /dt = 100 A/μs	-	12.7	-	nS
Q _{rr}	Reverse Recovery Charge		-	2.8	-	μC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 30 V Frequency = 1 MHz	-	1058	-	pF
C _{oss}	Output Capacitance		-	42	-	
C _{rss}	Reverse Transfer Capacitance		-	35	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} = 30 V, V _{GEN} = 10 V, R _G = 4.5 Ω, R _L = 3 Ω, I _{DS} = 5 A	-	7.4	-	nS
t _r	Turn-on Rise Time		-	26	-	
t _{d(off)}	Turn-off Delay Time		-	17	-	
t _f	Turn-off Fall Time		-	28	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} = 30 V, V _{GS} = 10 V, I _{DS} = 5 A	-	19	-	nC
Q _{gs}	Gate-Source Charge		-	5	-	
Q _{gd}	Gate-Drain Charge		-	2.6	-	

Notes :

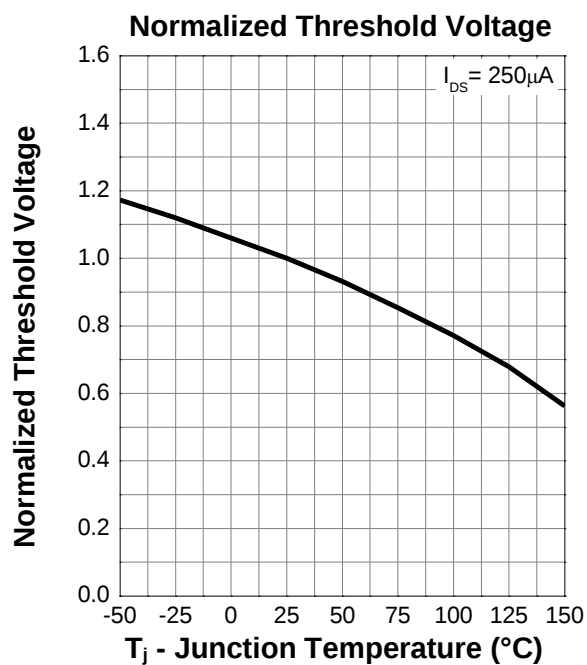
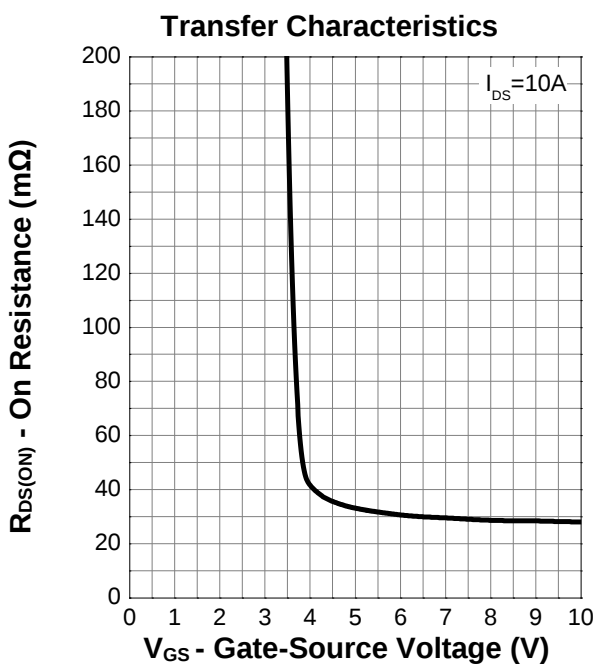
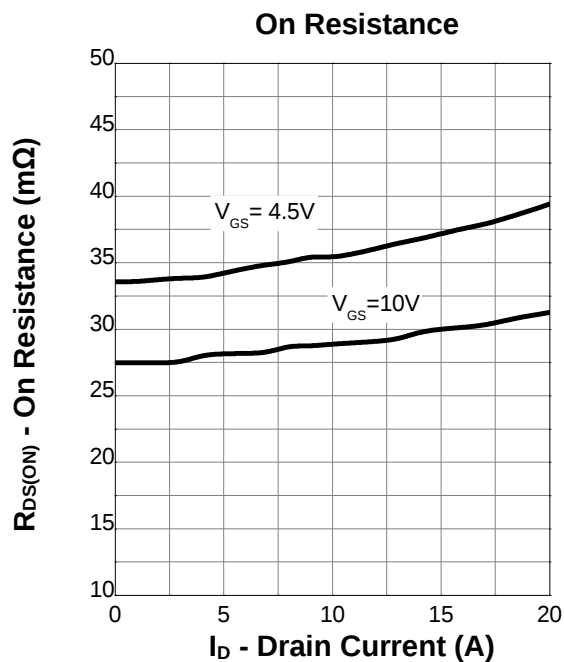
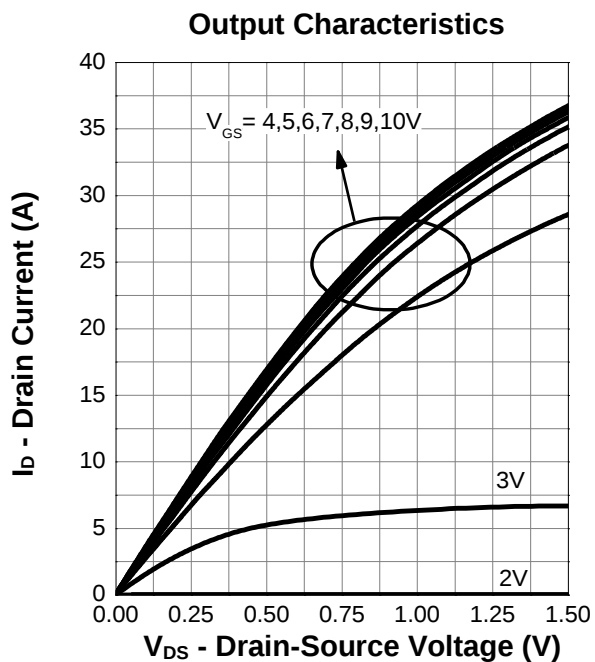
a : Pulse test ; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b : Guaranteed by design, not subject to production testing

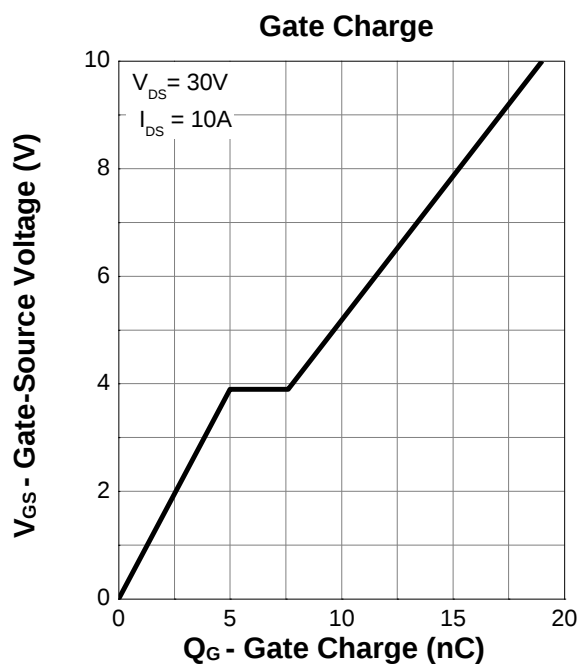
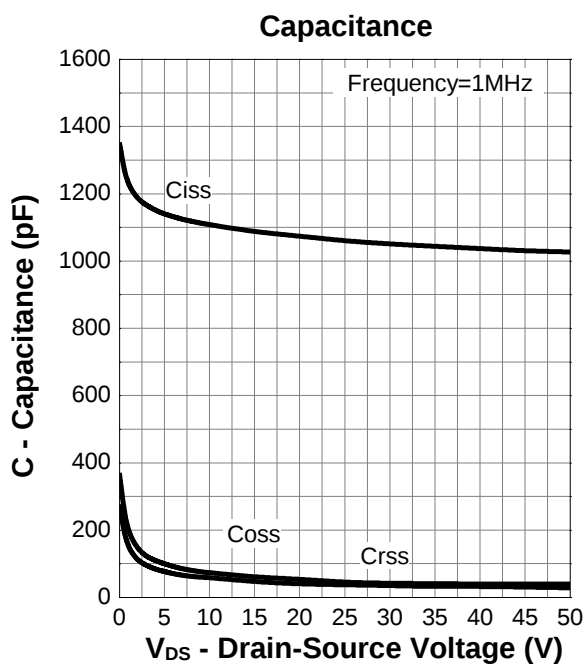
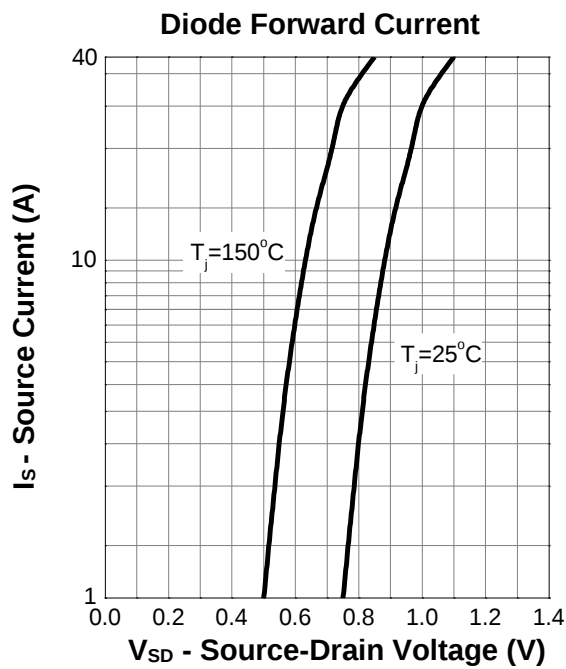
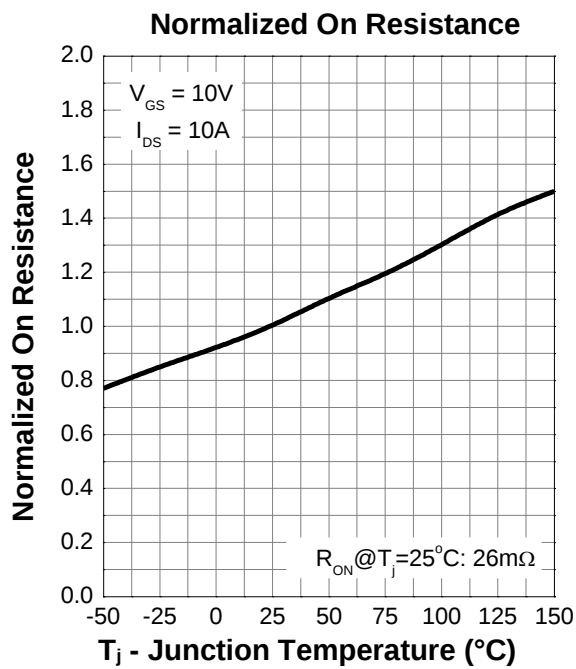
7. Typical Characteristics



7. Typical Characteristics (cont.)

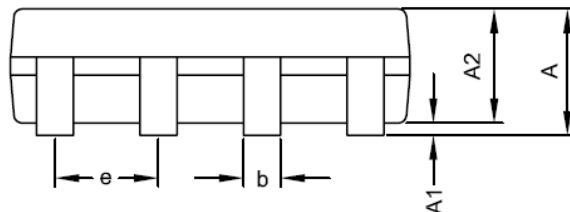
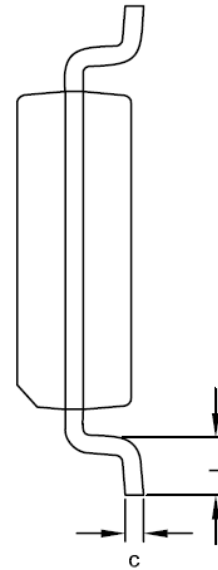
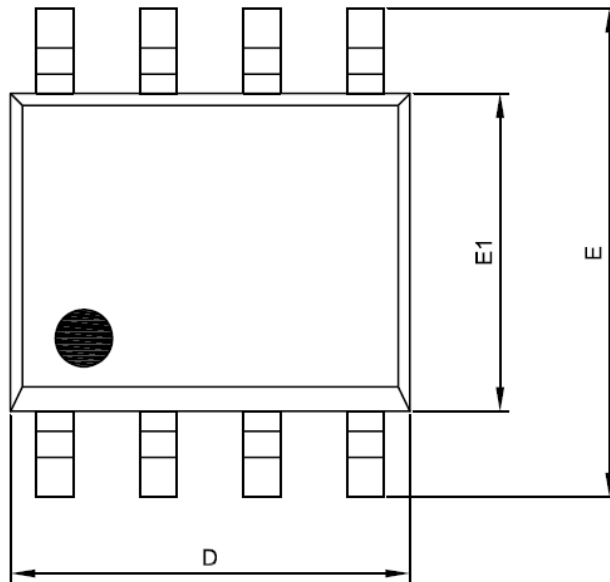


7. Typical Characteristics (cont.)



8. Package Dimensions

SOP- 8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes :

1. Jedec outline : MS-012AA
2. Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.