

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☒ Advanced trench cell design
- ☒ Super Trench
- ☒ Low Thermal Resistance

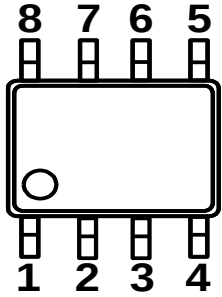
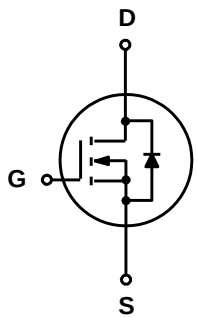
1.2 Applications

- ☒ Motor drivers
- ☒ DC - DC Converter

1.3 Quick reference

- ☒ $BV \geq 100\text{ V}$
- ☒ $P_{tot} \leq 2\text{ W}$
- ☒ $I_D \leq 12\text{ A}$
- ☒ $R_{DS(ON)} \leq 12\text{ m}\Omega @ V_{GS} = 10\text{ V}$
- ☒ $R_{DS(ON)} \leq 15\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1,2,3	Source(S)	 Top View SOP- 8L	
4	Gate(G)		
5,6,7,8	Drain(D)		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_C = 25\text{ }^{\circ}\text{C}$	-	100	V
V_{GS}	Gate-Source Voltage	$T_C = 25\text{ }^{\circ}\text{C}$	-	± 20	V
I_D^*	Drain Current	$T_C = 25\text{ }^{\circ}\text{C}, V_{GS} = 10\text{ V}$	-	12	A
		$T_C = 100\text{ }^{\circ}\text{C}, V_{GS} = 10\text{ V}$	-	8	A
$I_{DM}^{*,**}$	Pulsed Source Current	$T_C = 25\text{ }^{\circ}\text{C}, V_{GS} = 10\text{ V}$	-	40	A
P_{tot}^*	Total Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	-	35	W
T_{stg}	Storage Temperature		- 55	150	$^{\circ}\text{C}$
T_J	Junction Temperature		-	150	$^{\circ}\text{C}$
I_S	Diode Forward Current	$T_C = 25\text{ }^{\circ}\text{C}$	-	12	A
$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient		-	62.5	$^{\circ}\text{C} / \text{W}$

Notes :

- * Surface Mounted on 1 in² pad area, $t \leq 10\text{ sec}$
- ** Pulse width $\leq 10\text{ }\mu\text{s}$, duty cycle $\leq 1\%$
- *** Limited by bonding wire

4. Marking Information

Product Name	Marking
KJ1010S	1010 YWWXXX YWW: Date Code

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ1010S	SOP8			3000	

Note: KUAJIEXIN defines " Green " as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

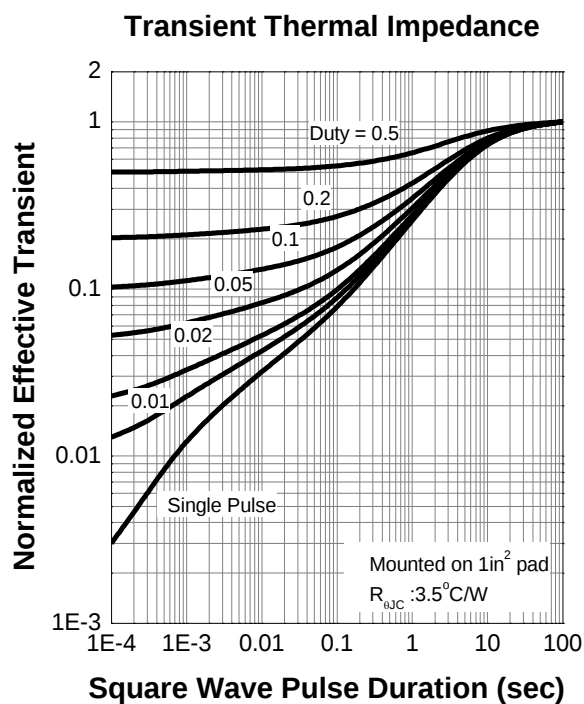
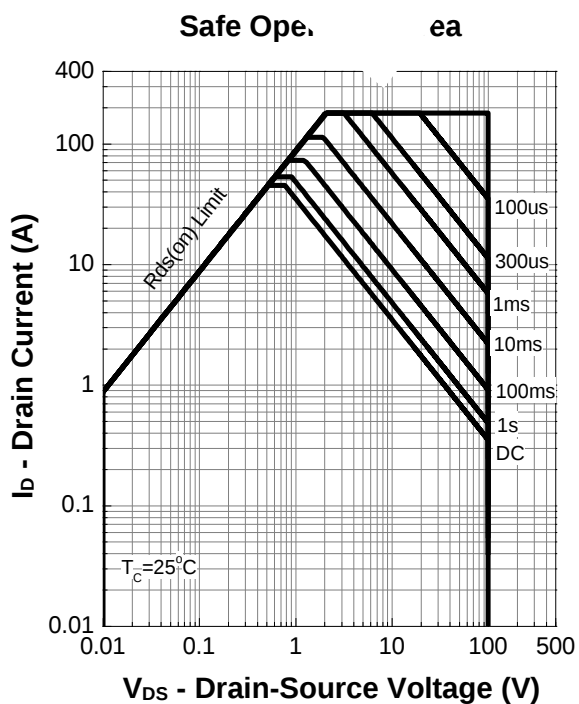
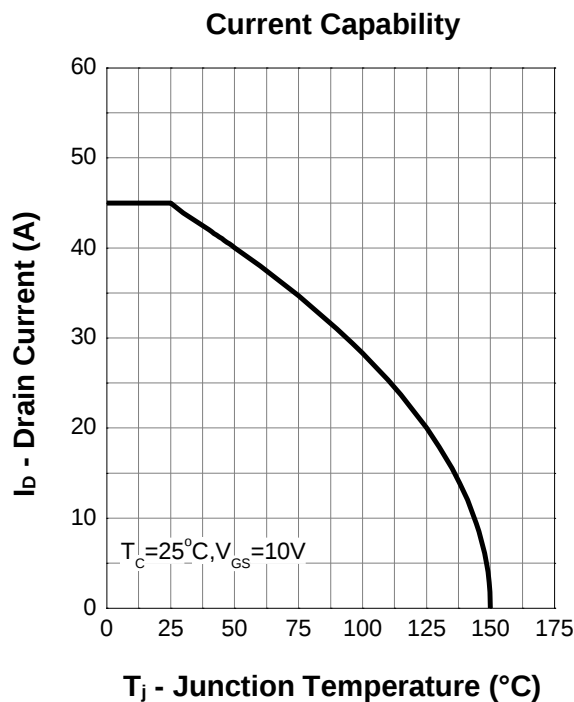
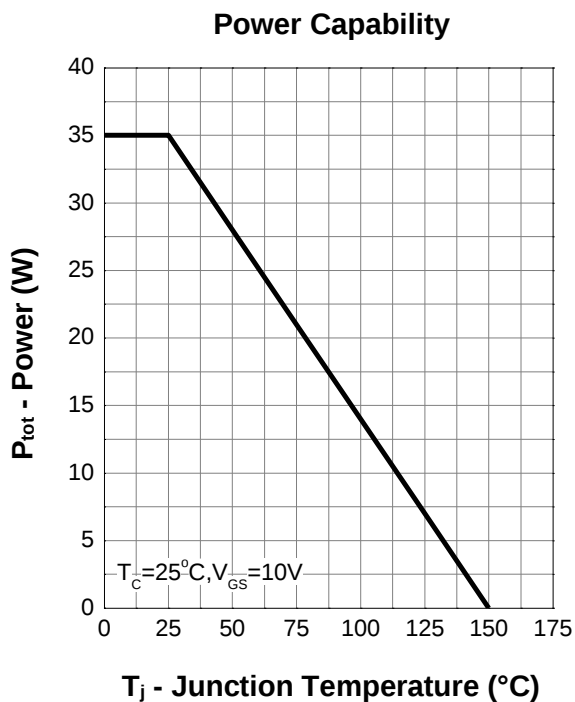
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	100	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	1.0	-	3.0	V
I _{DSS}	Zero Gate Voltage Source Current	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	μA
		T _J = 85 °C	-	-	30	μA
I _{GSS}	Gate Leakage Current	V _{GS} = ± 20 V, V _{DS} = 0 V	-	-	± 100	nA
R _{DS(ON)} ^a	Drain-Source On-State Resistance	V _{GS} = 10 V, I _D = 10 A	-	-	11	m Ω
		V _{GS} = 4.5 V, I _D = 10 A	-	-	15	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} = 10 A, V _{GS} = 0 V	-	-	1.3	V
t _{rr}	Reverse Recovery Time	I _{SD} = 10 A, dI _{SD} /dt = 100 A/μs	-	55	-	ns
Q _{rr}	Reverse Recovery Charge		-	70.7	-	nC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 30 V Frequency = 1 MHz	-	1707	-	pF
C _{oss}	Output Capacitance		-	790	-	
C _{rss}	Reverse Transfer Capacitance		-	68	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} = 50 V, V _{GEN} = 10 V, R _G = 4.5 Ω, R _L = 2.5 Ω, I _{DS} = 10 A	-	9.4	-	ns
t _r	Turn-on Rise Time		-	26	-	
t _{d(off)}	Turn-off Delay Time		-	23.6	-	
t _f	Turn-off Fall Time		-	41	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} = 50 V, V _{GS} = 10 V, I _{DS} = 10 A	-	28.7	-	nC
Q _{gs}	Gate-Source Charge		-	8.1	-	
Q _{gd}	Gate-Drain Charge		-	5.1	-	

Notes :

a : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2 %

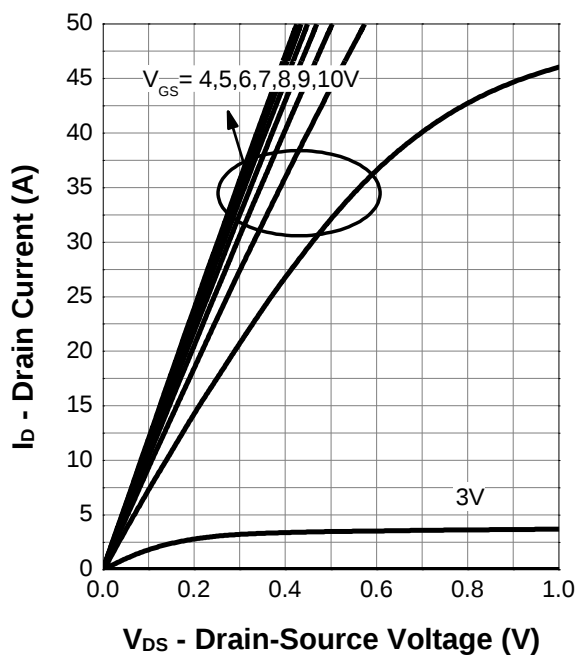
b : Guaranteed by design, not subject to production testing

7. Typical Characteristics (Cont.)

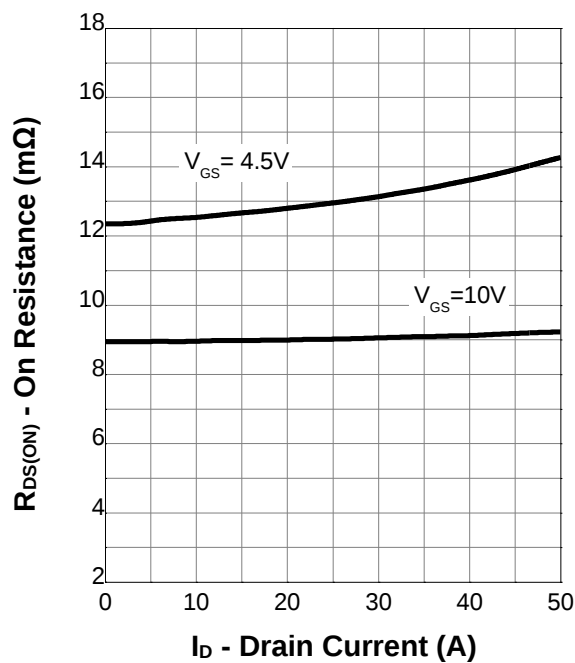


7. Typical Characteristics (Cont.)

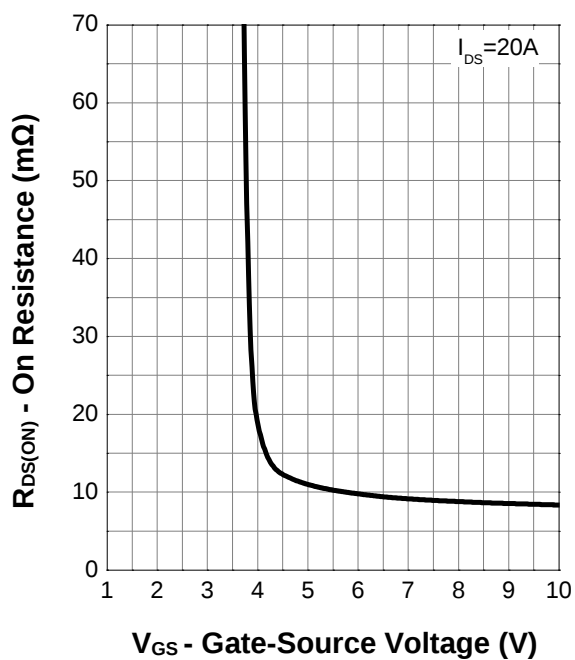
Output Characteristics



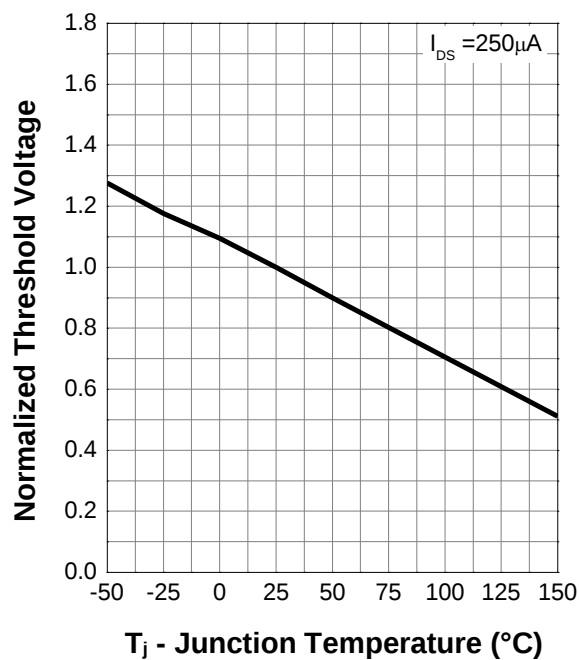
On Resistance



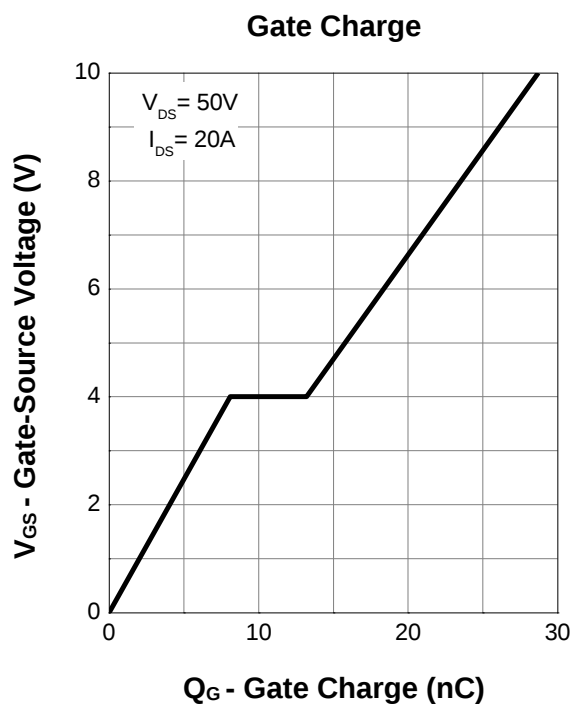
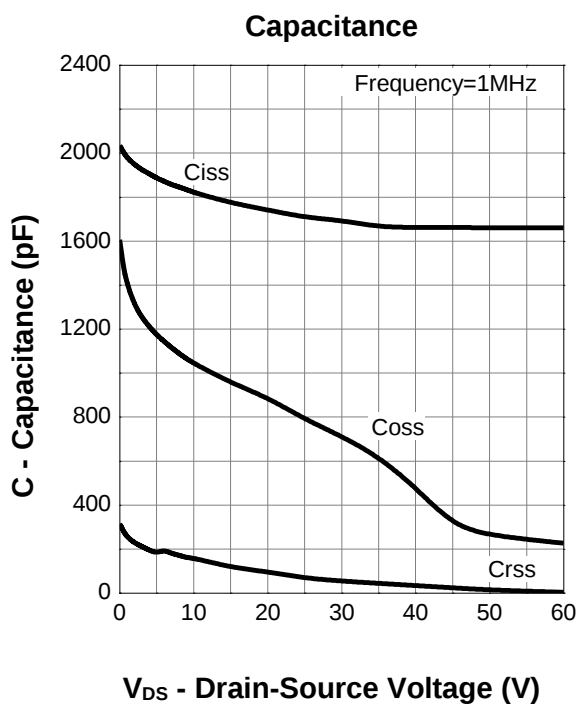
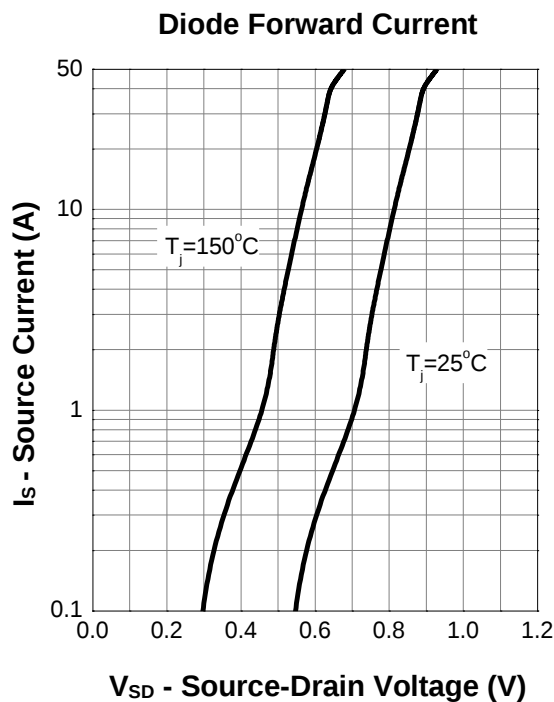
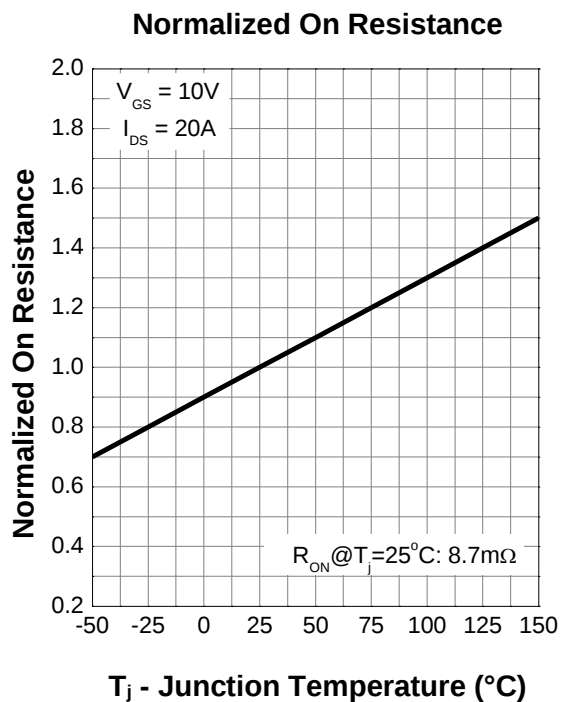
Transfer Characteristics



Normalized Threshold Voltage

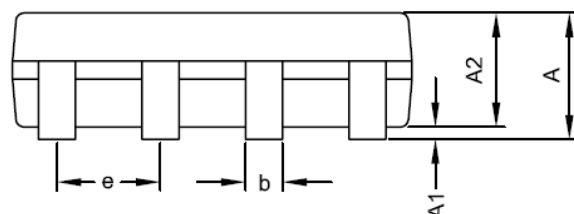
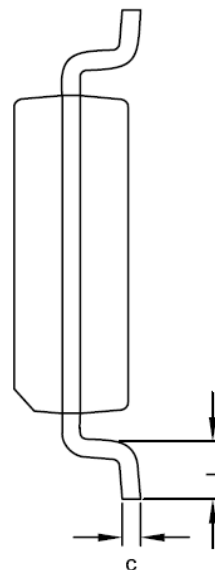
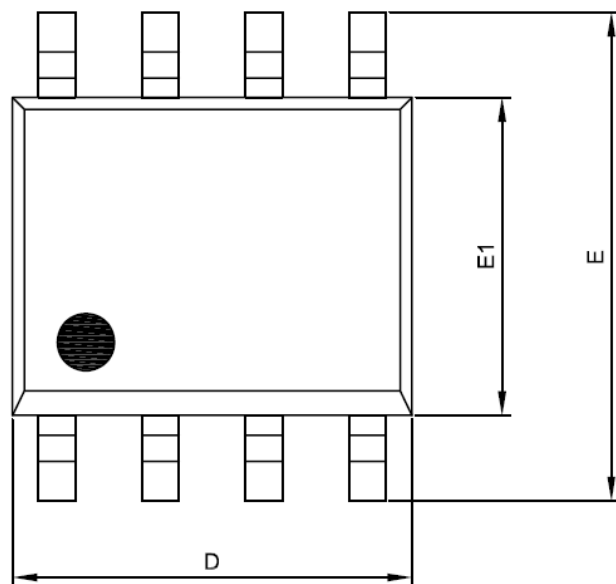


7. Typical Characteristics (Cont.)



8. Package Dimensions

SOP- 8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes :

1. Jedec outline : MS-012AA
2. Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.