

## Dual P-Channel Enhancement Mode MOSFET

### 1. Product Information

#### 1.1 Features

- Surface-mounted package
- Advanced trench cell design

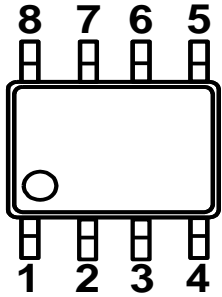
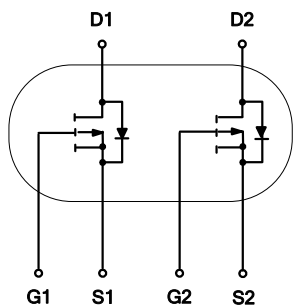
#### 1.2 Applications

- LED Display appliances
- High power inverter system
- LCDM appliances

#### 1.3 Quick reference

- $BV \geq -30\text{ V}$
- $R_{DS(ON)} \leq 55\text{ m}\Omega @ V_{GS} = -10\text{ V}$
- $P_{tot} \leq 2\text{ W}$
- $R_{DS(ON)} \leq 65\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
- $I_D \leq -6.3\text{ A}$

### 2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Source(S1)	 <p>Top View SOP- 8L</p>	
2	Gate(G1)		
3	Source(S2)		
4	Gate(G2)		
5,6	Drain(D2)		
7,8	Drain(D1)		



### 3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	Drain-Source Voltage	T <sub>A</sub> = 25 °C	- 30	-	V
V <sub>GS</sub>	Gate-Source Voltage	T <sub>A</sub> = 25 °C	-	± 20	V
I <sub>D</sub> *	Drain Current	T <sub>A</sub> = 25 °C, V <sub>GS</sub> = - 10 V	-	- 6.3	A
		T <sub>A</sub> = 100 °C, V <sub>GS</sub> = - 10 V	-	- 4	A
I <sub>DM</sub> **	Pulsed Drain Current	T <sub>A</sub> = 25 °C, V <sub>GS</sub> = - 10 V	-	- 25	A
P <sub>tot</sub>	Total Power Dissipation	T <sub>A</sub> = 25 °C	-	2	W
T <sub>stg</sub>	Storage Temperature		- 55	150	°C
T <sub>J</sub>	Junction Temperature		- 55	150	°C
I <sub>S</sub>	Diode Forward Current	T <sub>A</sub> = 25 °C	-	- 6.3	A
R <sub>θJA</sub> *	Thermal Resistance- Junction to Ambient		-	62.5	°C / W

Notes :

- \* Surface Mounted on 1 in<sup>2</sup> pad area, t ≤ 10 sec
- \*\* Pulse width ≤ 300 μs, duty cycle ≤ 2 %

### 4. Marking Information

Product Name	Marking
KJ4953S	<div style="display: inline-block; border: 1px solid black; padding: 2px;">4953 YWWXXX</div> YWW: Date Code

### 5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ4953S	SOP8			3000	

Note: KUAJIEXIN defines " Green " as lead-free ( RoHS compliant ) and halogen free ( Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C )



## 6. Electrical Characteristics ( $T_A=25\text{ }^\circ\text{C}$ Unless Otherwise Noted )

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\text{ }\mu\text{A}$	- 30	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\text{ }\mu\text{A}$	- 1.0	-	- 2.0	V
$I_{DSS}$	Drain Leakage Current	$V_{DS} = - 24\text{ V}, V_{GS} = 0\text{ V}$	-	-	- 1.0	$\mu\text{A}$
$I_{GSS}$	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA
$R_{DS(ON)}^a$	On-State Resistance	$V_{GS} = - 10\text{ V}, I_{DS} = - 6\text{ A}$	-	45	55	m $\Omega$
		$V_{GS} = - 4.5\text{ V}, I_{DS} = - 3\text{ A}$	-	55	65	
Diode Characteristics						
$V_{SD}^a$	Diode Forward Voltage	$I_{SD} = - 6\text{ A}, V_{GS} = 0\text{ V}$	-	-	- 1.3	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = - 6\text{ A}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	38	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	17	-	nC
Dynamic Characteristics <sup>b</sup>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = - 15\text{ V}$ Frequency = 1 MHz	-	750	-	pF
$C_{oss}$	Output Capacitance		-	115	-	
$C_{riss}$	Reverse Transfer Capacitance		-	75	-	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = - 15\text{ V}, V_{GEN} = - 10\text{ V},$ $R_G = 4.5\text{ }\Omega, R_L = 2.5\text{ }\Omega,$ $I_{DS} = - 6\text{ A}$	-	7	-	ns
$t_r$	Turn-on Rise Time		-	3	-	
$t_d(off)$	Turn-off Delay Time		-	30	-	
$t_f$	Turn-off Fall Time		-	12	-	
Gate Charge Characteristics <sup>b</sup>						
$Q_g$	Total Gate Charge	$V_{DS} = - 15\text{ V}, V_{GS} = - 10\text{ V},$ $I_{DS} = - 6\text{ A}$	-	9.5	-	nC
$Q_{gs}$	Gate-Source Charge		-	2	-	
$Q_{gd}$	Gate-Drain Charge		-	3	-	

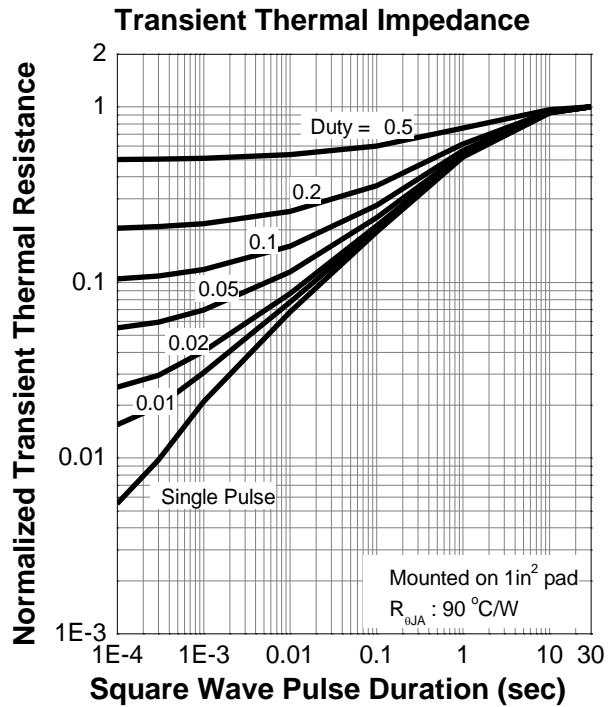
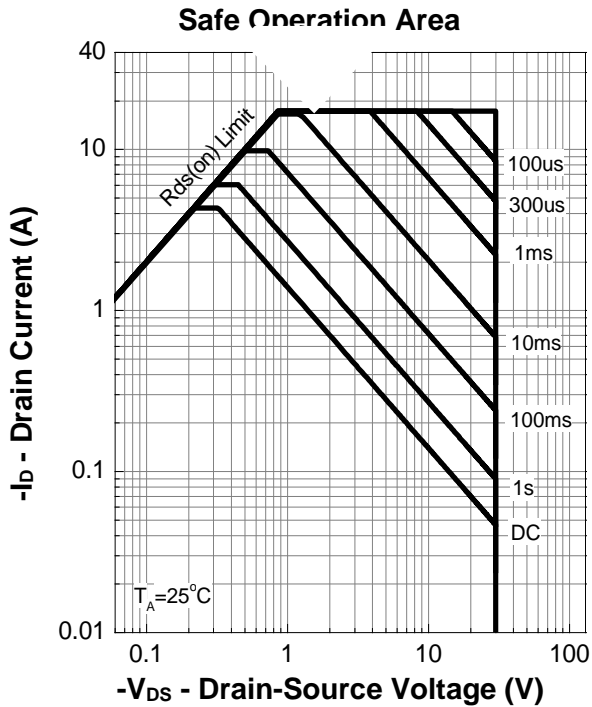
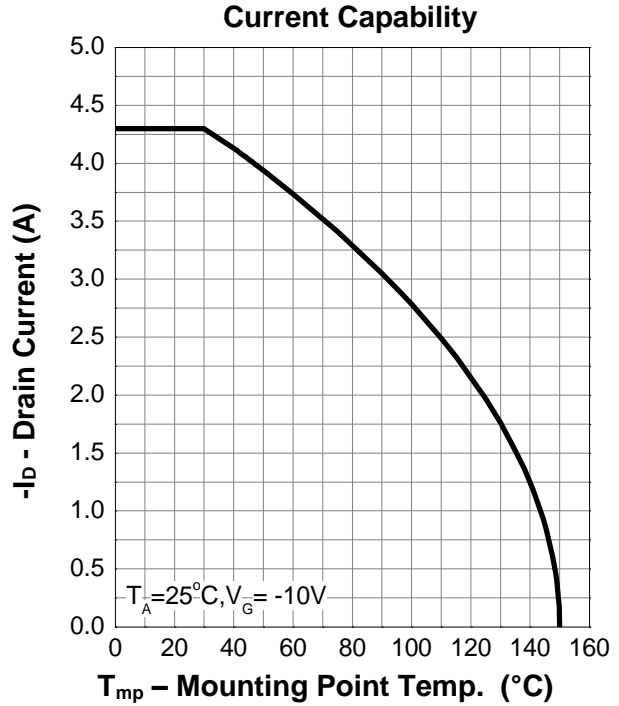
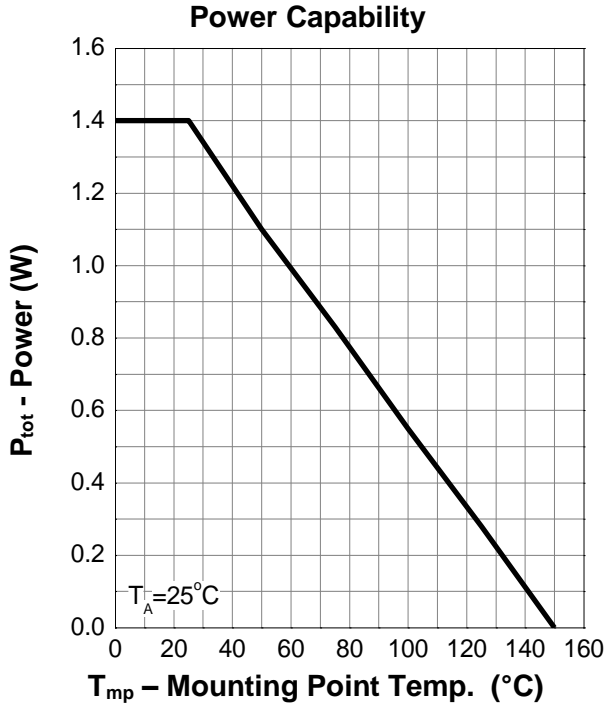
Notes :

a : Pulse test ; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$

b : Guaranteed by design, not subject to production testing

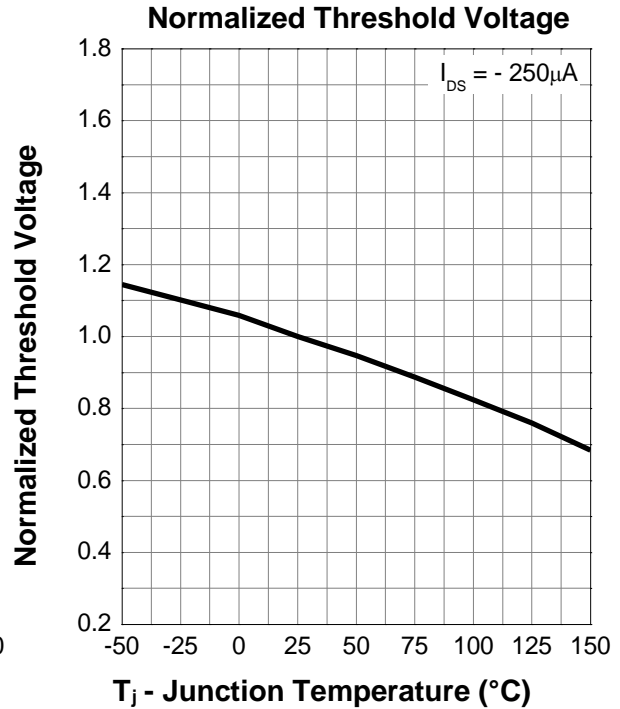
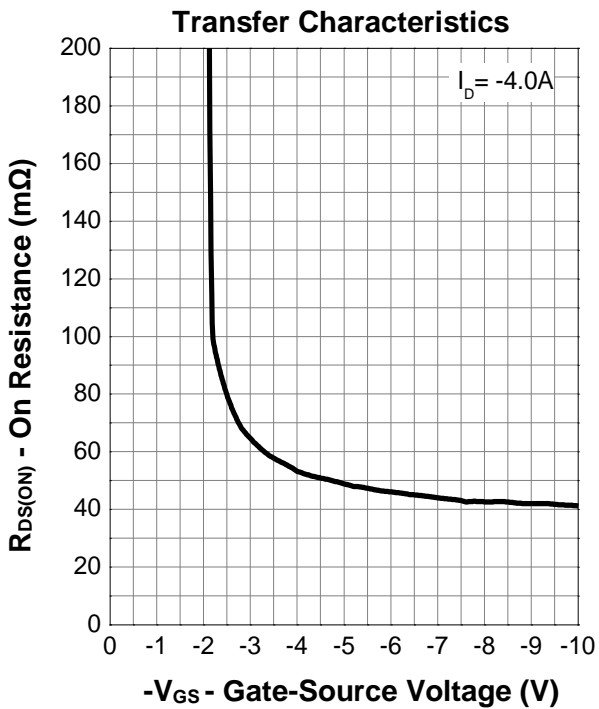
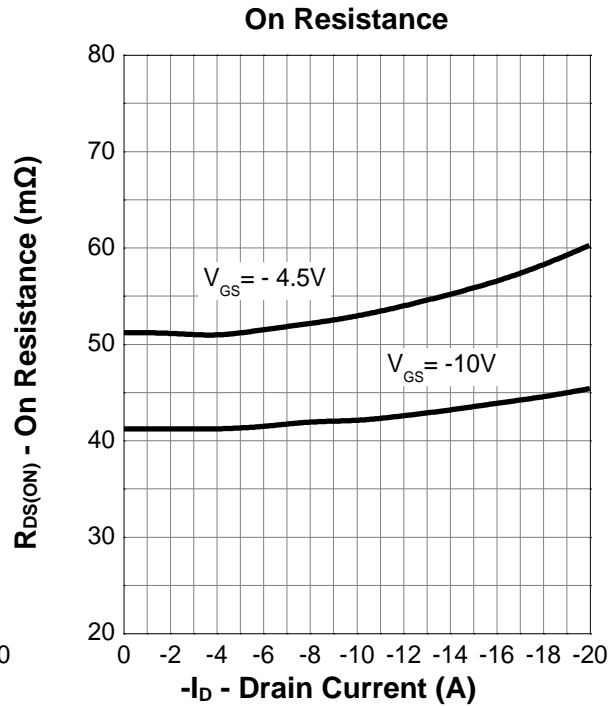
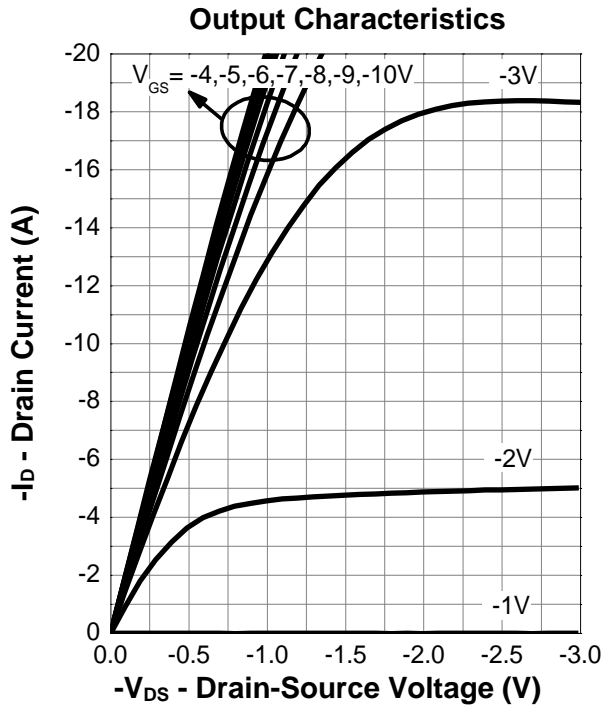


### 7. Typical Characteristics



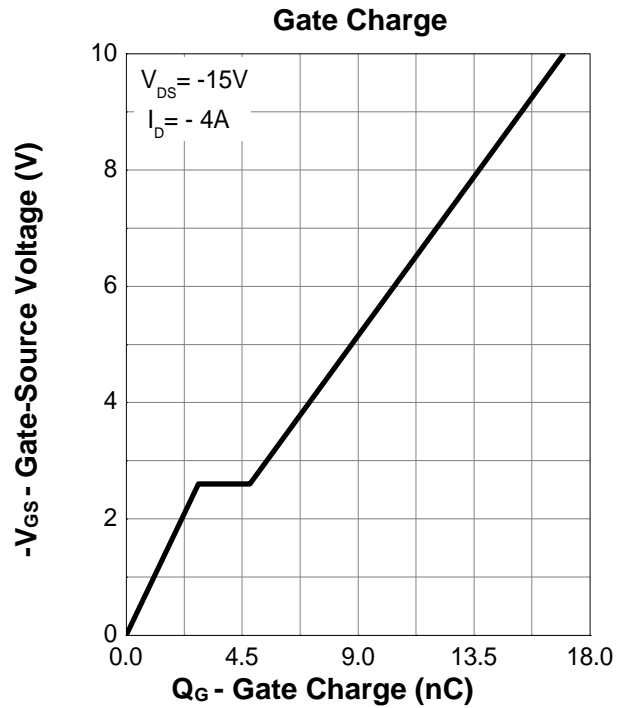
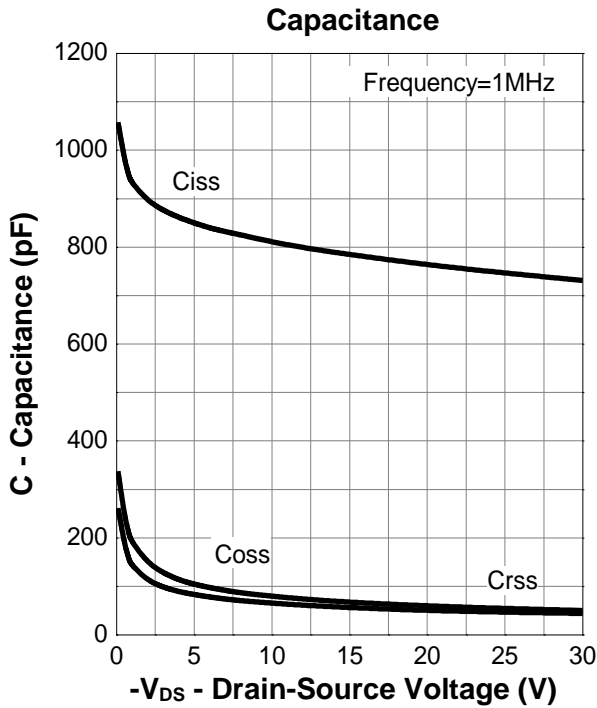
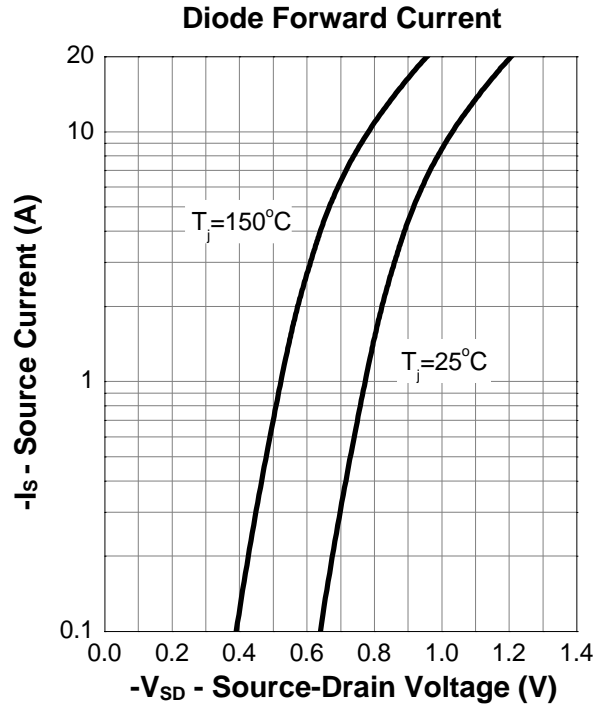
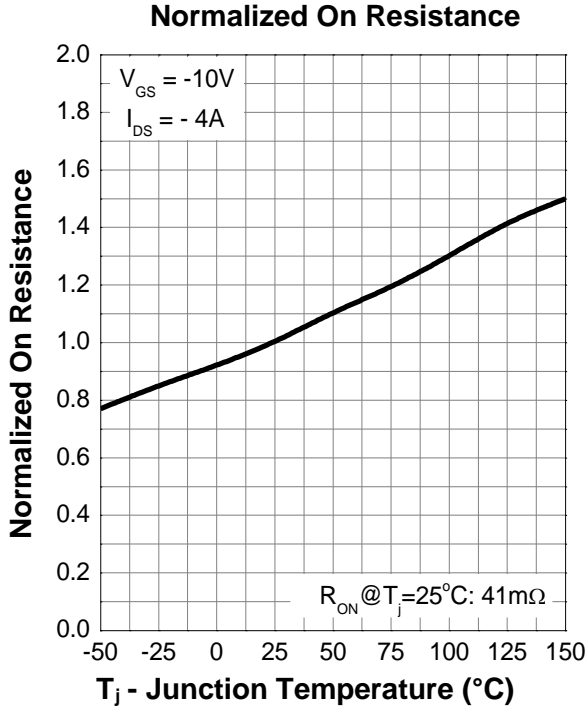


### 7. Typical Characteristics ( cont. )





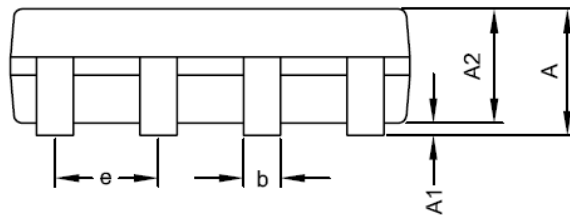
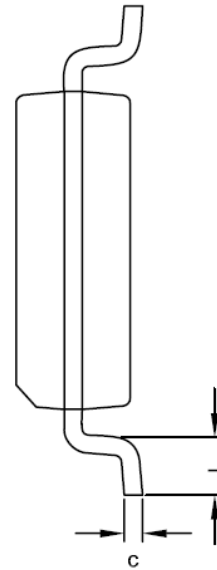
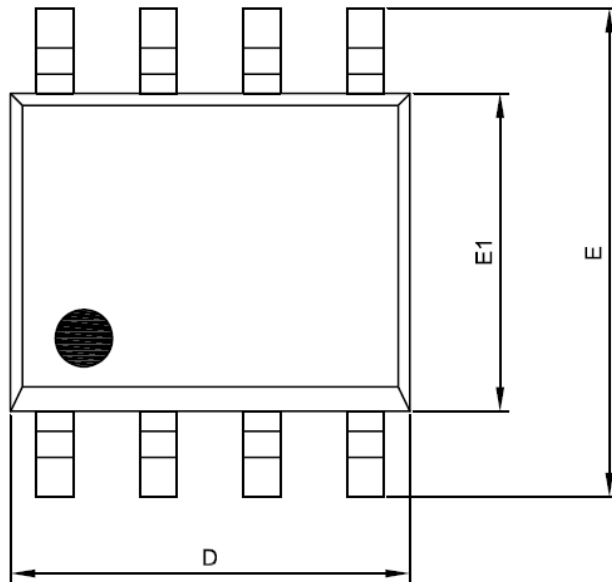
### 7. Typical Characteristics ( cont. )





### 8. Package Dimensions

SOP- 8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes :

1. Jedec outline : MS-012AA
2. Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.