

P-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☒ Surface-mounted package
- ☒ Low gate charge

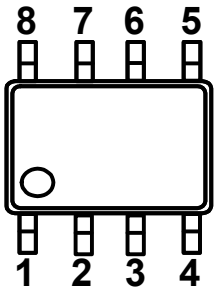
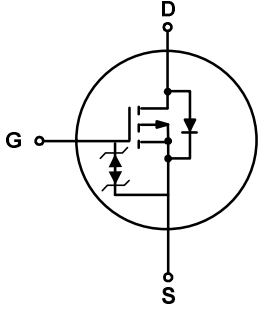
1.2 Applications

- ☒ Motor driver appliances
- ☒ Adapter appliances
- ☒ High power inverter system

1.3 Quick reference

- ☒ $BV \geq -40\text{ V}$
- ☒ $P_{\text{tot}} \leq 2\text{ W}$
- ☒ $I_D \leq -5.7\text{ A}$
- ☒ $R_{\text{DS(ON)}} \leq 55\text{ m}\Omega @ V_{\text{GS}} = -10\text{ V}$
- ☒ $R_{\text{DS(ON)}} \leq 80\text{ m}\Omega @ V_{\text{GS}} = -4.5\text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1,2,3	Source	 Top View SOP- 8L	
4	Gate		
5,6,7,8	Drain		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_A = 25\text{ }^{\circ}\text{C}$	- 40	-	V
V_{GS}	Gate-Source Voltage	$T_A = 25\text{ }^{\circ}\text{C}$	-	± 20	V
I_D^*	Drain Current (DC)	$T_A = 25\text{ }^{\circ}\text{C}, V_{GS} = -10\text{ V}$	-	- 5.7	A
		$T_A = 100\text{ }^{\circ}\text{C}, V_{GS} = -10\text{ V}$		- 3	A
I_{DM}^{***}	Drain Current (Pulsed)	$T_A = 25\text{ }^{\circ}\text{C}, V_{GS} = -10\text{ V}$	-	- 18.8	A
P_{tot}^*	Total Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$	-	2	W
T_{stg}	Storage Temperature		- 55	150	$^{\circ}\text{C}$
T_J	Junction Temperature		-	150	$^{\circ}\text{C}$
$R_{\theta JC}^*$	Thermal Resistance- Junction to Case		-	3.5	$^{\circ}\text{C} / \text{W}$
$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient		-	62.5	$^{\circ}\text{C} / \text{W}$

Notes :

* Surface Mounted on 1 in² pad area, $t \leq 10\text{ sec}$

** Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

*** limited by bonding wire

4. Marking Information

Product Name	Marking
KJ06P04S	06P04 YWWXXX YWW: Date Code

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ06P04S	SOP8			3000	

Note: KUAJIEXIN defines “ Green ” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

**快捷****KJ06P04S****6. Electrical Characteristics** ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

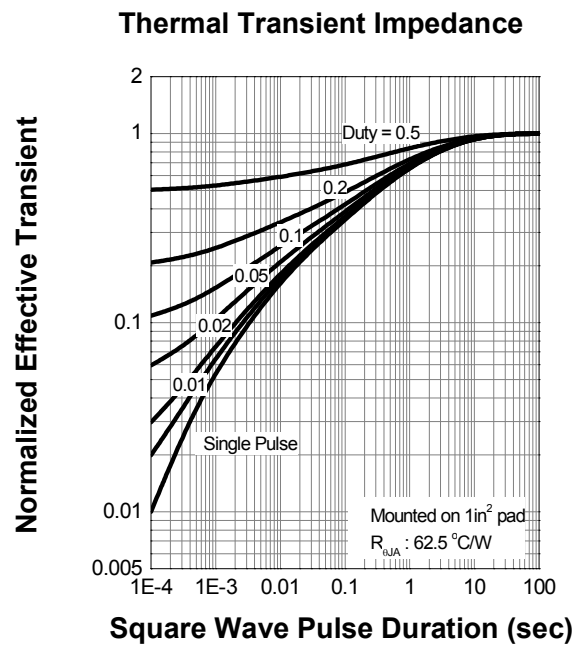
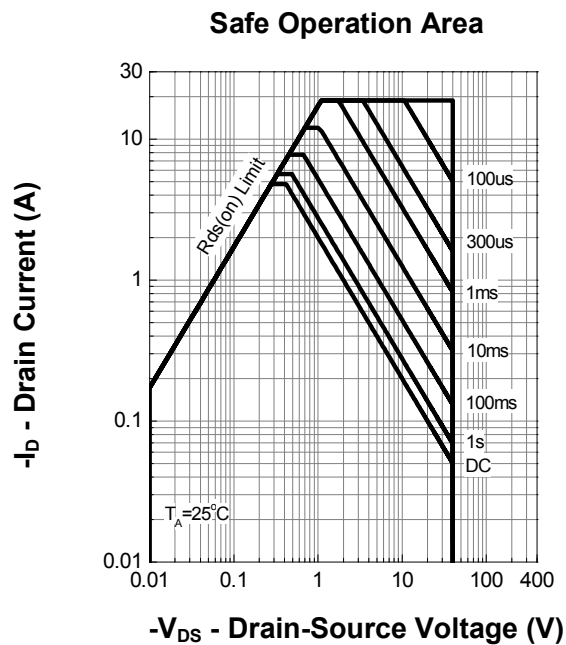
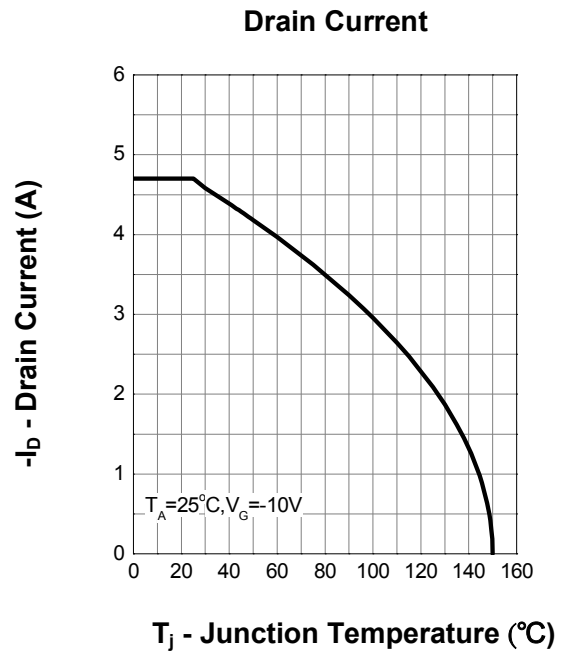
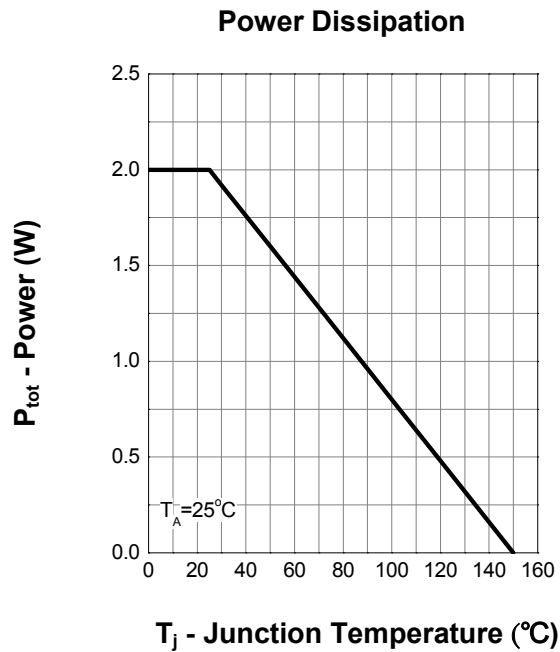
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _{DS} = - 250 μA	- 40	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = - 250 μA	- 1	-	- 2	V
I _{DSS}	Drain Leakage Current	V _{DS} = - 32 V, V _{GS} = 0 V	-	-	- 1	μA
I _{GSS}	Gate Leakage Current	V _{GS} = ± 20 V, V _{DS} = 0 V	-	-	± 8	μA
R _{DS(ON)} ^a	Channel On-State Resistance	V _{GS} = - 10 V, I _D = - 4 A	-	48	55	mΩ
	Channel On-State Resistance	V _{GS} = - 4.5 V, I _D = - 2 A	-	71	80	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} = - 4 A, V _{GS} = 0 V	-	-	- 1.3	V
t _{rr}	Reverse Recovery Time	I _{SD} = - 4 A, dI _{SD} / dt = 100 A / μs	-	11	-	nS
Q _{rr}	Reverse Recovery Charge		-	6.9	-	nC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS</}				

Notes :

a : Pulse test ; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

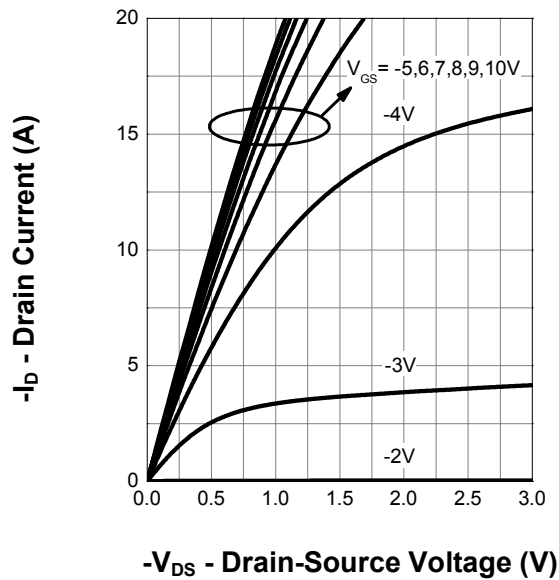
b : Guaranteed by design, not subject to production testing

7. Typical Characteristics

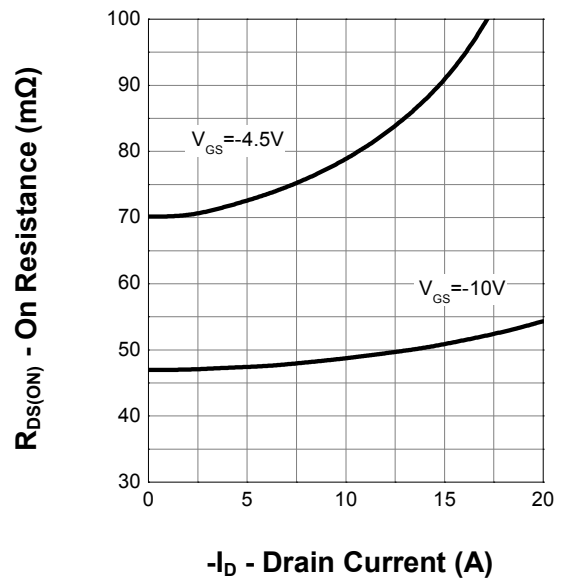


7. Typical Characteristics (cont.)

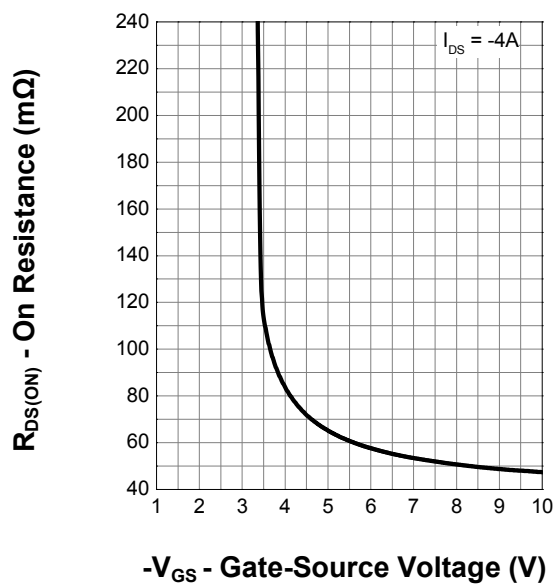
Output Characteristics



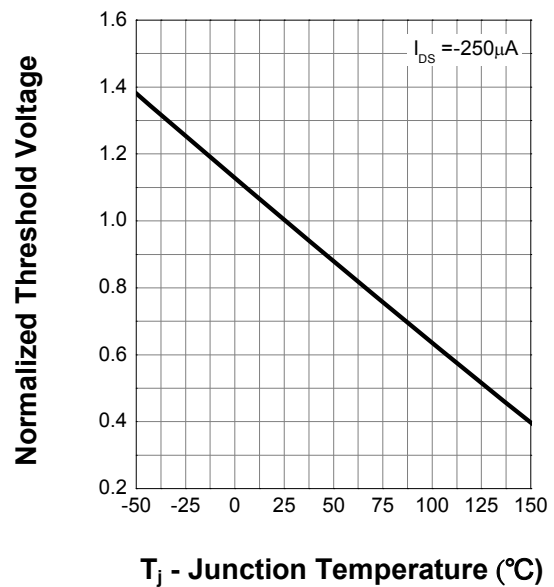
Drain-Source On Resistance



Transfer Characteristics

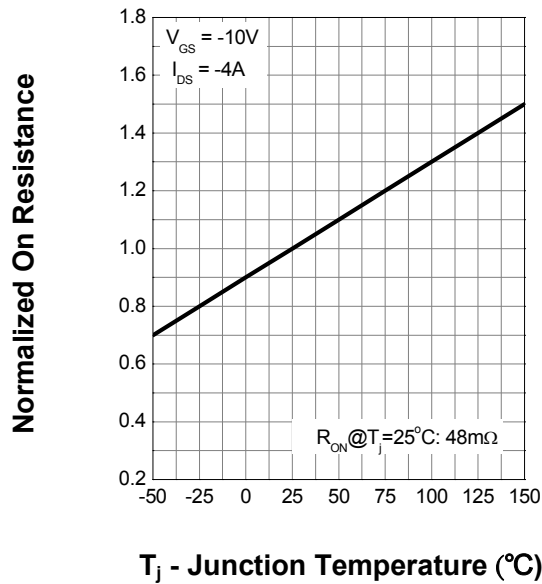


Gate Threshold Voltage

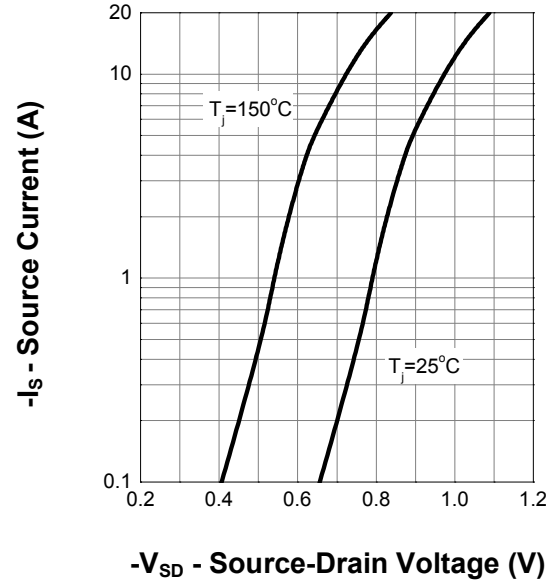


7. Typical Characteristics (cont.)

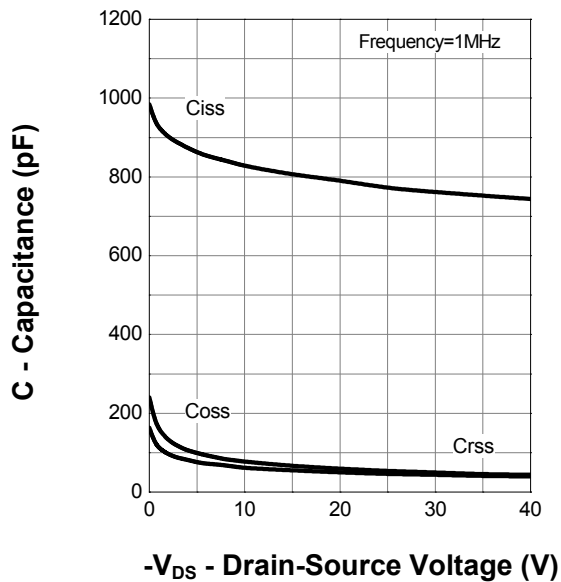
Drain-Source On Resistance



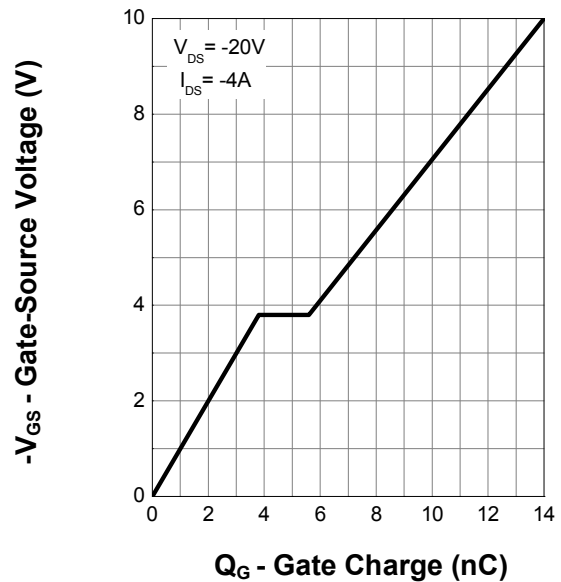
Source-Drain Diode Forward



Capacitance

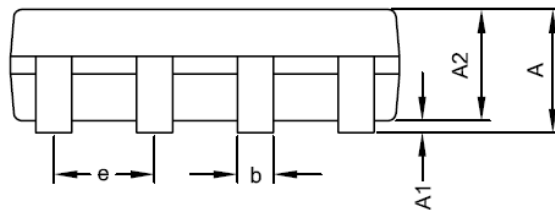
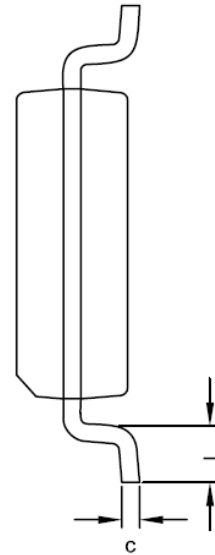
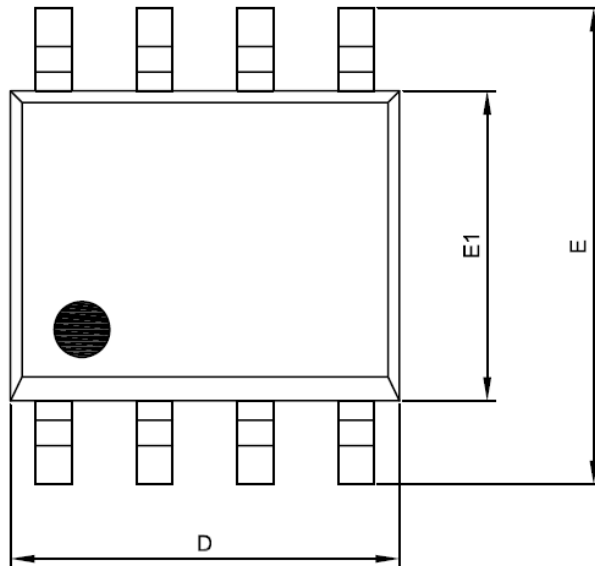


Gate Charge



8. Package Dimensions

SOP- 8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes :

1. Jedec outline : MS-012AA
2. Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.