N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Advanced trench cell design
- ☑ Lead free product is acquired
- ☑ Excellent RDS(ON) and Low Gate Charge

1.2 Applications

- ☑ PWM applications
- ☑ Power management
- ☑ Load Switch

1.3 Quick reference

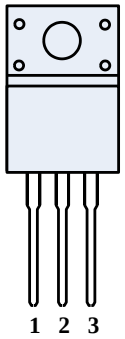
- ☑ BV ≧ 200 V
- ☑ P_{tot} ≦ 375 W
- ☑ I_D ≦ 75 A
- ☑ $R_{DS(ON)}$ ≦ 20 mΩ @ V_{GS} = 10 V

2. Pin Description

Pin	Description
1	Gate (G)
2	Drain (D)
3	Source (S)

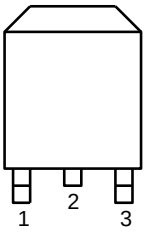
KJ75N20C

TO220 Top View

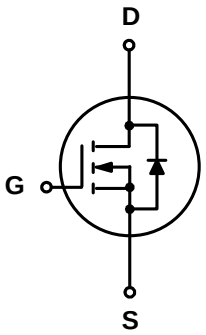


KJ75N20D

TO263 Top View



Symbol



3. Marking Information

Product Name	Marking
KJ75N20C KJ75N20D	75N20 YWWXXX YWW: Date Code

4. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ75N20C	TO-220			1000	
KJ75N20D	TO-263			800	

5. Absolute Maximum Ratings (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-to-Source Voltage	200	V
I_D@TA=25℃	Continuous Drain Current V_{GS} @ 10V	75	A
I_D@TA=70℃	Continuous Drain Current V_{GS} @ 10V	52	A
I_{DM} [a1]	Pulsed Drain Current (pulse width limited by TJM)	300	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy	300	mJ
E_{Ar}[a1]	Avalanche Energy, Repetitive	75	mJ
I_{AR} [a1]	Avalanche Current	45	A
dv/dt [a2]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	375	W
T_J，T_{stg}	Operating Junction and Storage Temperature Range	150，– 55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.45	℃/ W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	60	℃/ W

Electrical Characteristics (T_A=25℃ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	200	220	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=200V, V_{GS}=0V, T_a=25℃	--	--	1.0	μA
		V_{DS}=200V, V_{GS}=0V, T_a=125℃	--	--	100	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+20V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-20V	--	--	-100	nA
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V, I_D=40A	--	17	20	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=VGS, I_D=250μA	3.6	--	5.0	V
g_{fs}	Forward Trans conductance	V_{DS}=25V, I_D=40A	50	65	--	S
R_g	Gate Resistance	V_{GS}=0V V_{DS} open f=1.0MHz	--	--	1.3	Ω
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=25V f=1.0MHz	--	7500	--	pF
C_{oss}	Output Capacitance		--	500	--	pF
C_{rss}	Reverse Transfer Capacitance		--	210	--	pF
$t_{d(ON)}$	Turn-on Delay Time	I_D=40A, V_{DS}=50V V_{GS}=10V, R_g=2.5Ω	--	45	--	ns
t_r	Rise Time		--	70	--	ns
$t_{d(OFF)}$	Turn-Off Delay Time		--	110	--	ns
t_f	Fall Time		--	90	--	ns
Q_g	Total Gate Charge	I_D=40A, V_{DD}=100V, V_{GS}=10V	--	85	--	nC
Q_{gs}	Gate to Source Charge		--	15	--	nC
Q_{gd}	Gate to Drain (“Miller”) Charge		--	25	--	nC
I_{SD}	Continuous Source Current (Body Diode)		--	--	75	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	300	A
V_{SD}	Diode Forward Voltage	I_S=40A, V_{GS}=0V	--	--	1.2	V
t_{rr}	Reverse Recovery Time	I_S=30A, T_j=25℃, V_{DD}=50V dI$_F$/dt=100A/μs, V_{GS}=0V	--	110	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.55	--	uC

Note:
1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2 OZ copper.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3. The E_{AS} data shows Max. rating. The test condition is T_J = 25°C, L = 0.3mH, R_G = 25Ω, V_{DD}=50V, V_{GS}=10V a2
4. The I_{SD}=40A, di/dt≤100A/us, V_{DD}≤B_{VDS}, Start T_J=25℃
5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

6. Typical Characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

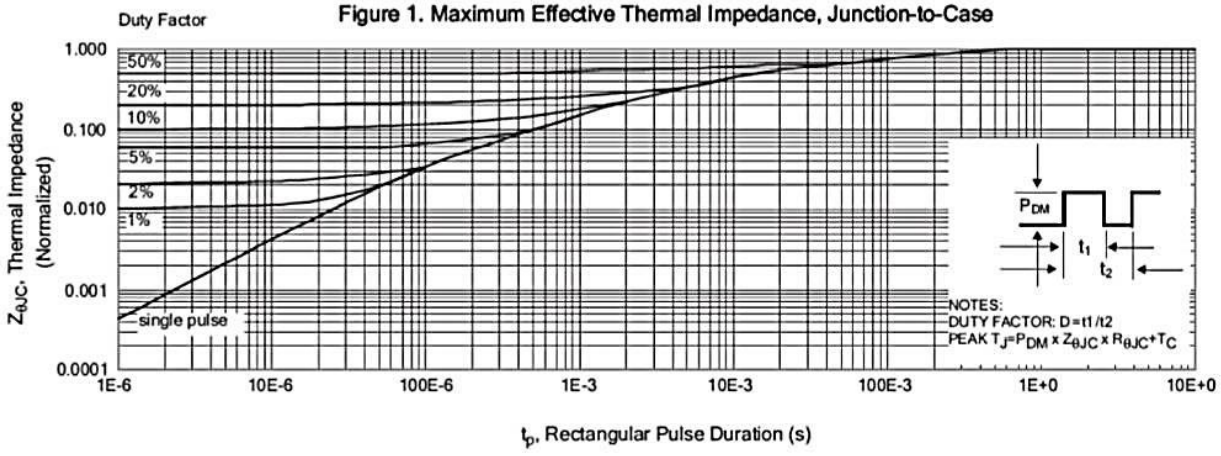


Figure 2 . Max. Power Dissipation vs Case Temperature

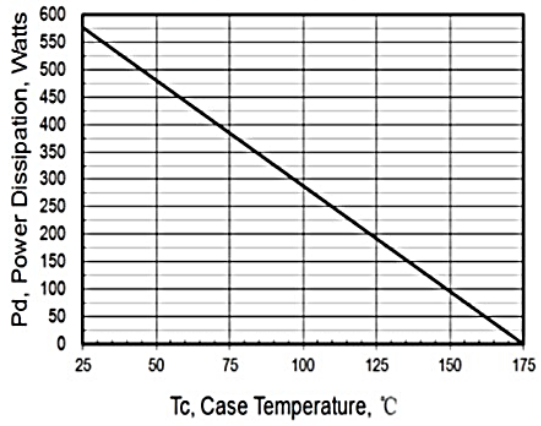


Figure 3 .Maximum Continuous Drain Current vs Tc

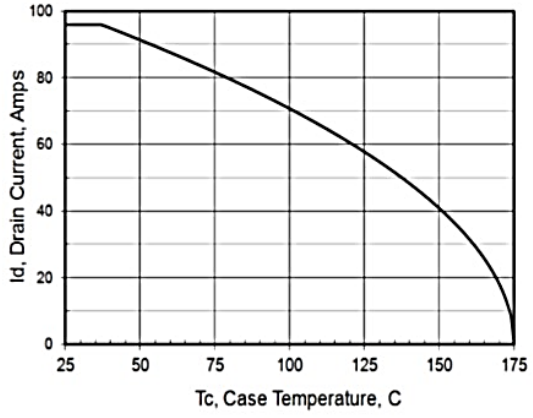


Figure 4. Typical Output Characteristics

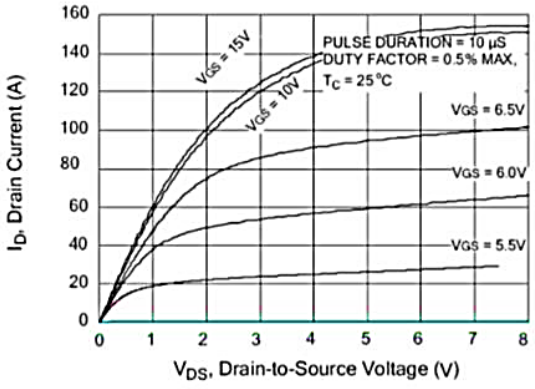


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

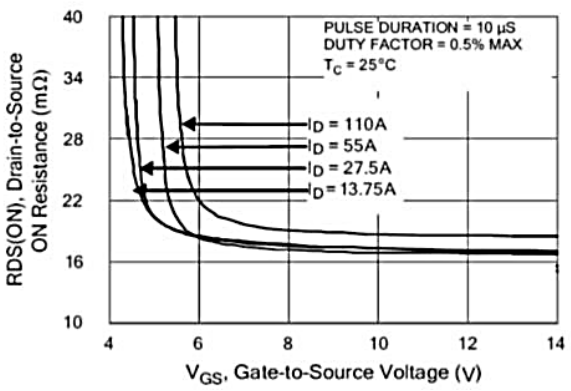


Figure 6. Peak Current Capability

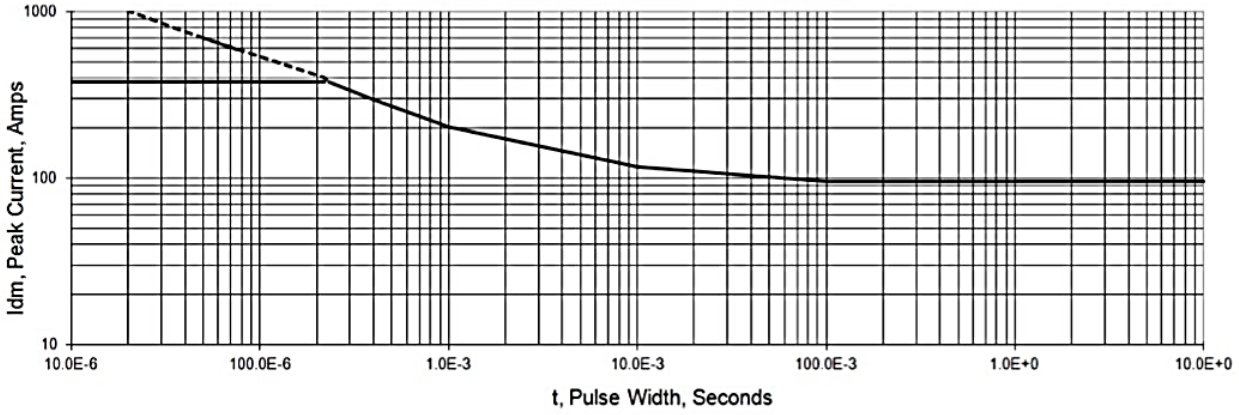


Figure 7. Typical Transfer Characteristics

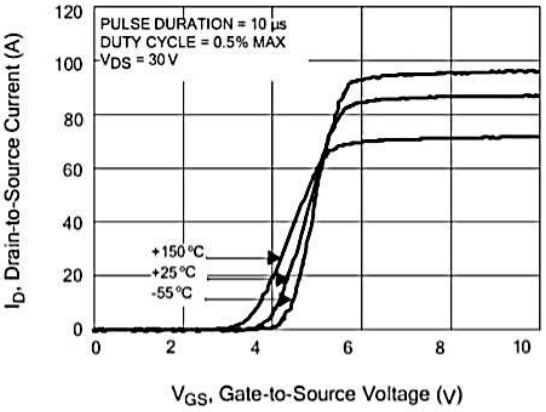


Figure 8. Unclamped Inductive Switching Capability

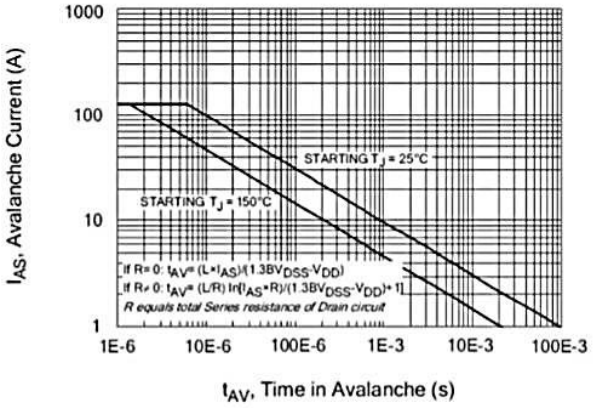


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

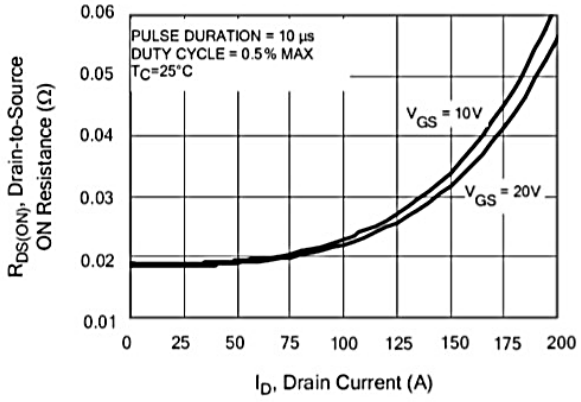


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

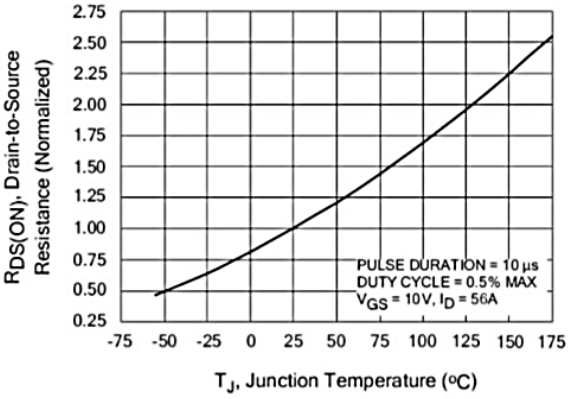


Figure 11. Typical Breakdown Voltage vs Junction Temperature

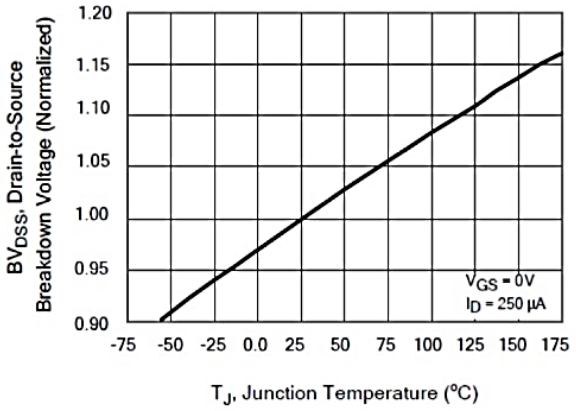


Figure 12. Typical Threshold Voltage vs Junction Temperature

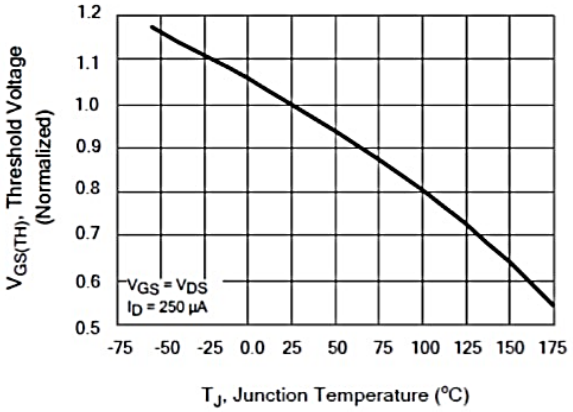


Figure 13 . Maximum Safe Operating Area

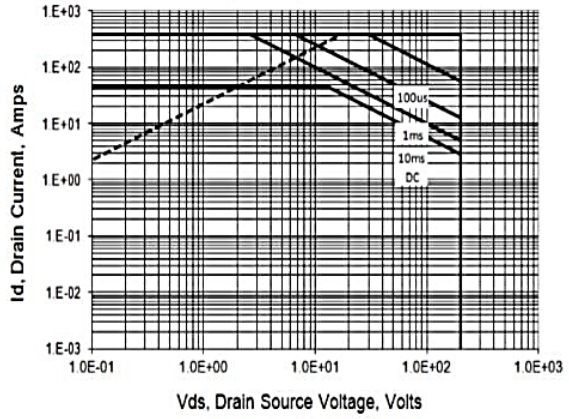


Figure 14. Capacitance vs Vds

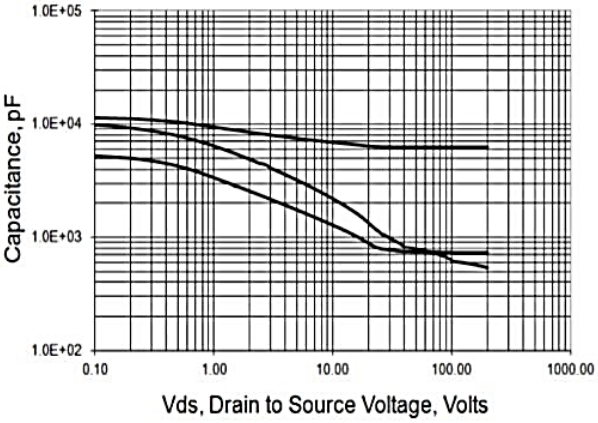


Figure 15 .Typical Gate Charge

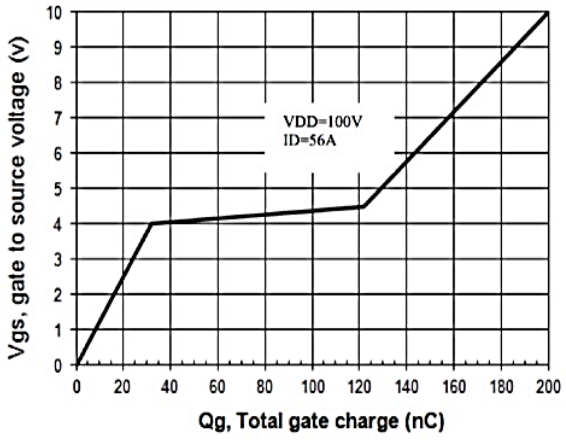
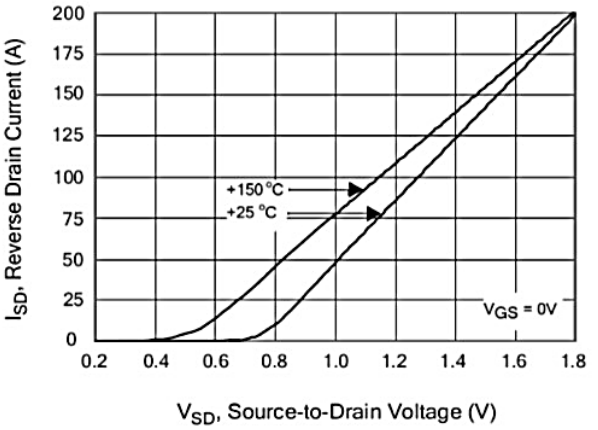
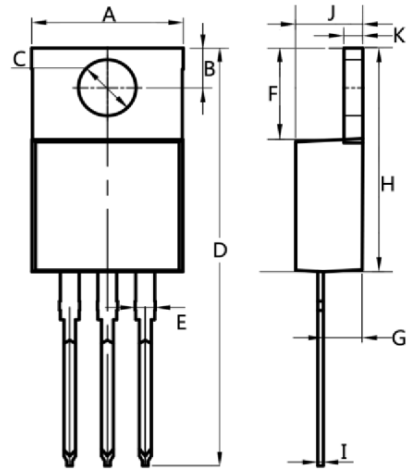


Figure 16. Typical Body Diode Transfer Characteristics



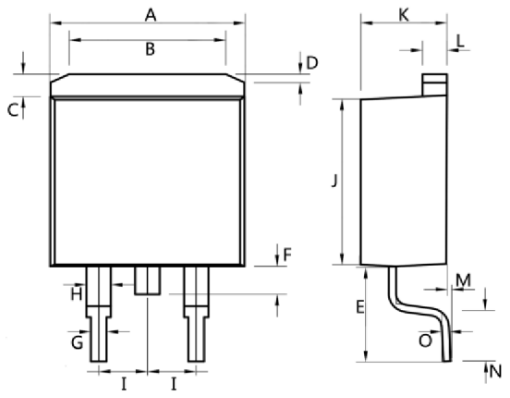
7.Package Dimensions

TO-220AB



Dim.	Min.	Max.
A	10.0	10.4
B	2.5	3.0
C	3.5	4.0
D	28.0	30.0
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
H	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4
All Dimensions in millimeter		

TO-263



Dim.	Min.	Max.
A	10.0	10. 5
B	7.25	7.75
C	1.3	1.5
D	0.55	0.75
E	5.0	6.0
F	1.4	1.6
G	0.75	0.95
H	1.15	1.35
I	Typ 2.54	
J	8.4	8.6
K	4.4	4.6
L	1.25	1.45
M	0.02	0.1
N	2.4	2.8
O	0.35	0.45
All Dimensions in millimeter		