

Dual P-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☒ Surface-mounted package
- ☒ Low gate charge

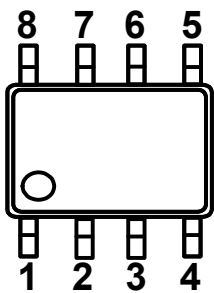
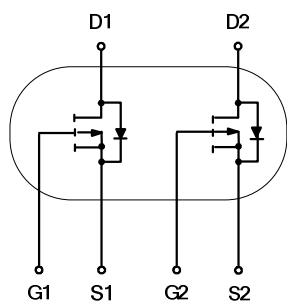
1.2 Applications

- ☒ Motor driver appliances
- ☒ Adapter appliances
- ☒ High power inverter system

1.3 Quick reference

- ☒ $BV \geq -30\text{ V}$
- ☒ $P_{\text{tot}} \leq 2.2\text{ W}$
- ☒ $I_D \leq -10\text{ A}$
- ☒ $R_{\text{DS(ON)}} \leq 18\text{ m}\Omega @ V_{\text{GS}} = -10\text{ V}$
- ☒ $R_{\text{DS(ON)}} \leq 28\text{ m}\Omega @ V_{\text{GS}} = -4.5\text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Source(S1)	 Top View SOP8	
2	Gate(G1)		
3	Source(S2)		
4	Gate(G2)		
5,6	Drain(D2)		
7,8	Drain(D1)		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_A = 25\text{ }^{\circ}\text{C}$	-	- 30	V
V_{GS}	Gate-Source Voltage	$T_A = 25\text{ }^{\circ}\text{C}$	-	± 20	V
I_D^*	Drain Current (DC)	$T_A = 25\text{ }^{\circ}\text{C}, V_{GS} = -10\text{ V}$	-	- 10	A
		$T_A = 100\text{ }^{\circ}\text{C}, V_{GS} = -10\text{ V}$		- 5.5	A
I_{DM}^{***}	Drain Current (Pulsed)	$T_A = 25\text{ }^{\circ}\text{C}, V_{GS} = -10\text{ V}$	-	- 34	A
P_{tot}^*	Total Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$	-	2.2	W
T_{stg}	Storage Temperature		- 55	150	$^{\circ}\text{C}$
T_J	Junction Temperature		-	150	$^{\circ}\text{C}$
I_S	Diode Forward Current	$T_C = 25\text{ }^{\circ}\text{C}$	-	- 10	A
$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient		-	56.3	$^{\circ}\text{C} / \text{W}$

4. Marking Information

Product Name	Marking
KJ15P03DS	15P03D YWWXXX YWW: Date Code

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
K J15P03DS	SOP8			3000	

6. Electrical Characteristics ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

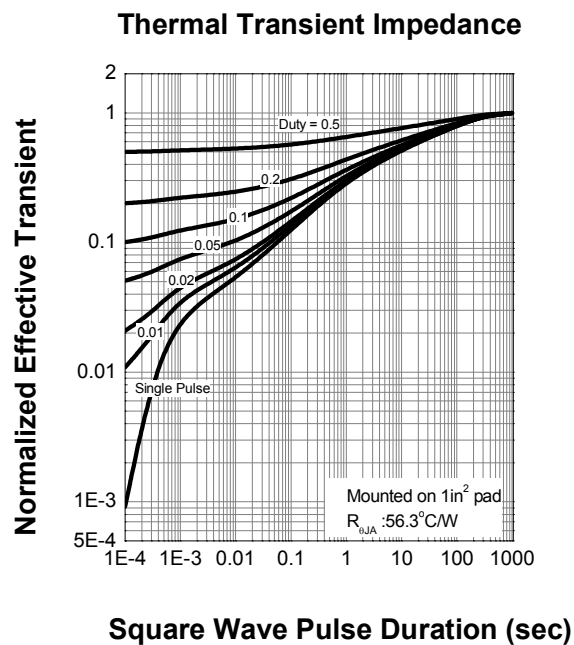
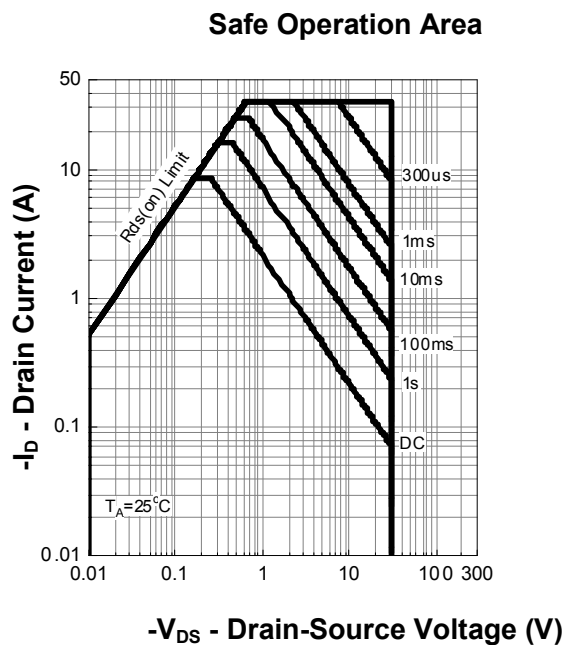
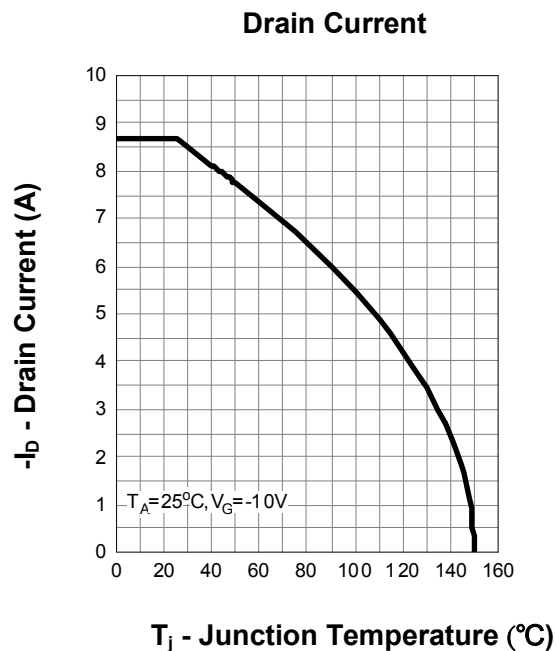
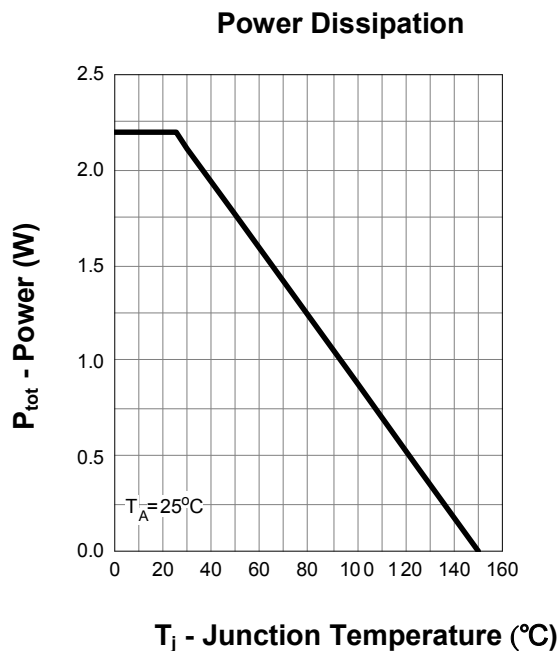
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _{DS} = - 250 μA	- 30	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = - 250 μA	- 1	-	- 2	V
I _{DSS}	Drain Leakage Current	V _{DS} = - 24V, V _{GS} = 0 V	-	-	- 1	μA
I _{GSS}	Gate Leakage Current	V _{GS} = ± 20 V, V _{DS} = 0 V	-	-	± 100	nA
R _{DS(ON)} ^a	Channel On-State Resistance	V _{GS} = - 10 V, I _D = - 5A	-	14.5	18	mΩ
	Channel On-State Resistance	V _{GS} = - 4.5 V, I _D = -3A	-	23.5	28	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} = - 5A, V _{GS} = 0 V	-	-	- 1.3	V
t _{rr}	Reverse Recovery Time	I _{SD} = - 5A, dI _{SD} / dt = 100 A / μs	-	12	-	nS
Q _{rr}	Reverse Recovery Charge		-	6.2	-	nC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = - 15V Frequency = 1 MHz	-	1953	-	pF
C _{oss}	Output Capacitance		-	175	-	
C _{rss}	Reverse Transfer Capacitance		-	146	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} = - 15V, V _{GEN} = - 10 V, R _G = 3.9 Ω, R _L = 3Ω, I _{DS} = - 5A	-	5.7	-	nS
t _r	Turn-on Rise Time		-	15	-	
t _{d(off)}	Turn-off Delay Time		-	117	-	
t _f	Turn-off Fall Time		-	40	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{GS} = - 10 V, V _{DS} = - 15V, I _{DS} = - 5A	-	33	-	nC
Q _{gs}	Gate-Source Charge		-	8.4	-	
Q _{gd}	Gate-Drain Charge		-	3.7	-	

Notes :

a : Pulse test ; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

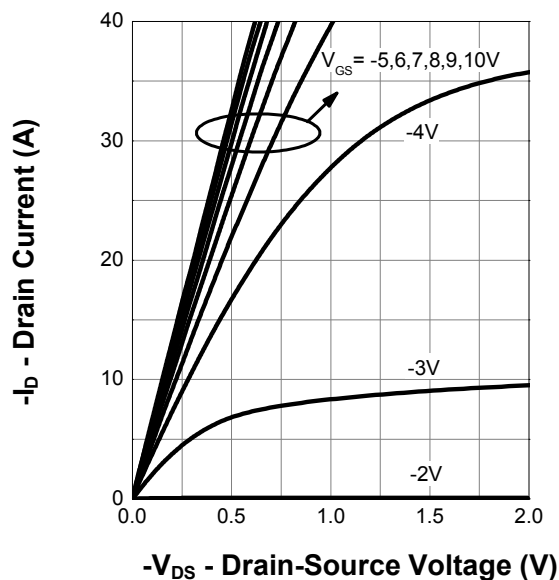
b : Guaranteed by design, not subject to production testing

7. Typical Characteristics

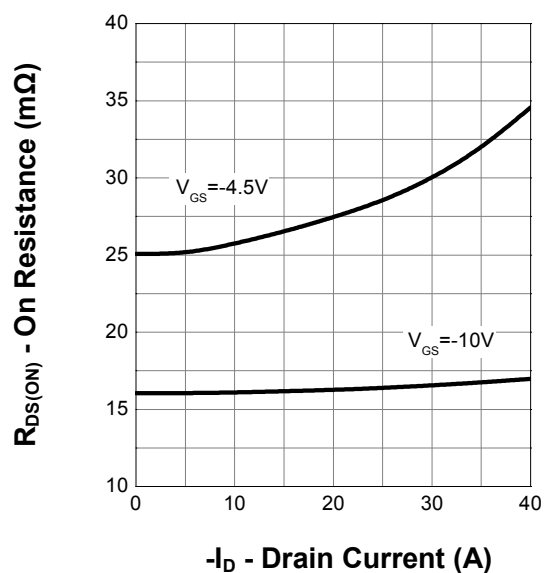


7. Typical Characteristics (cont.)

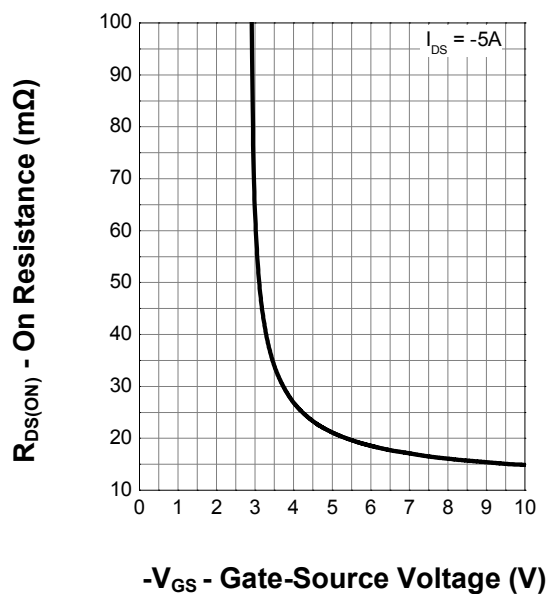
Output Characteristics



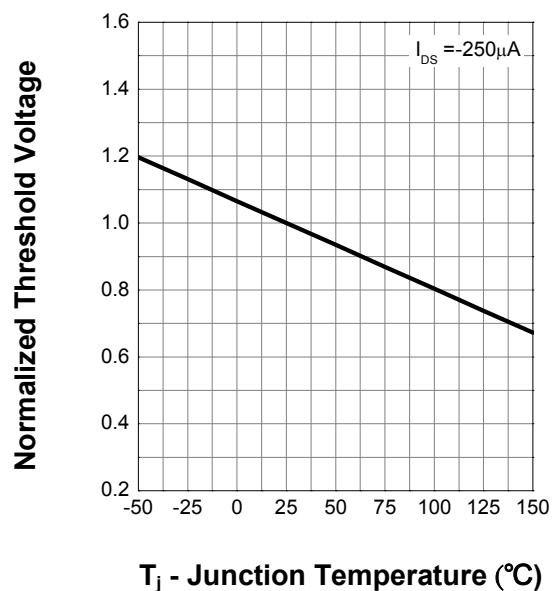
Drain-Source On Resistance



Transfer Characteristics

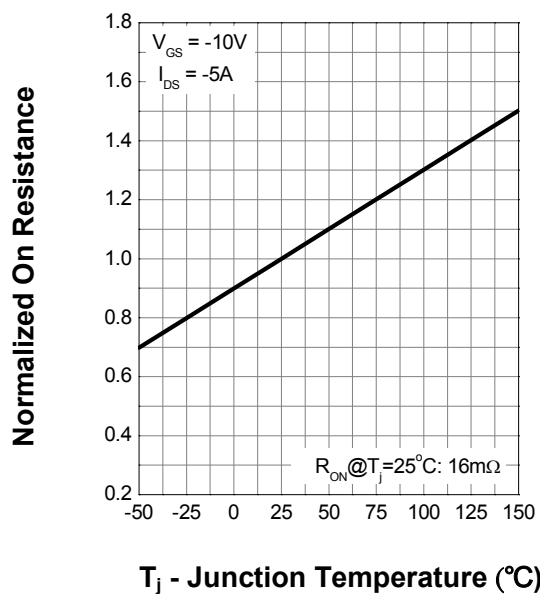


Gate Threshold Voltage

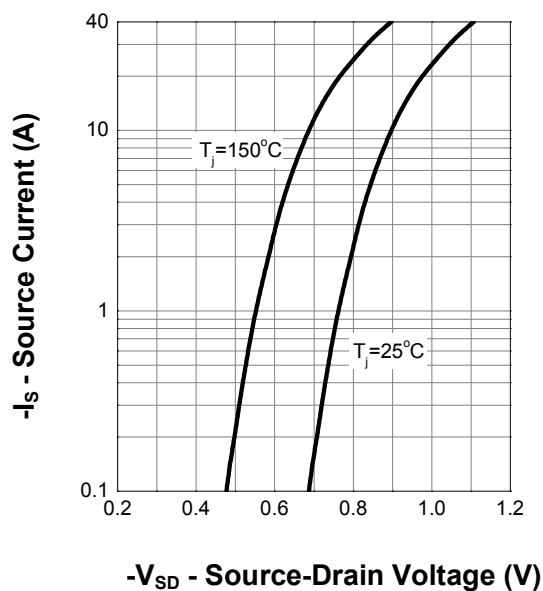


7. Typical Characteristics (cont.)

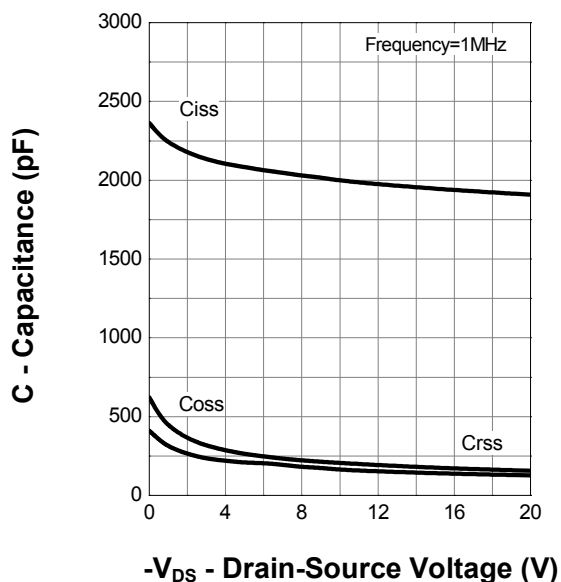
Drain-Source On Resistance



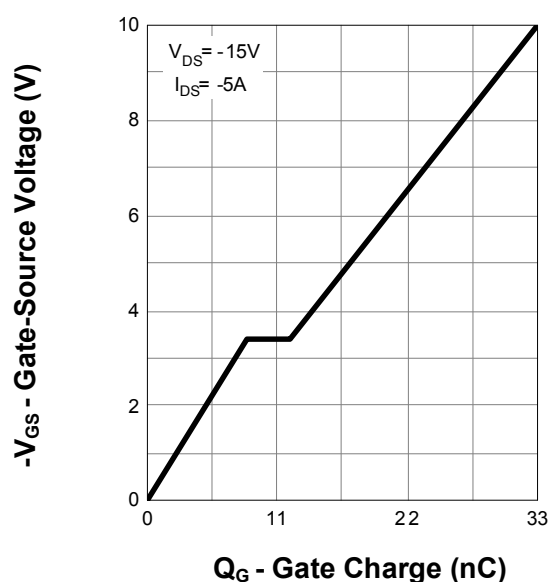
Source-Drain Diode Forward



Capacitance

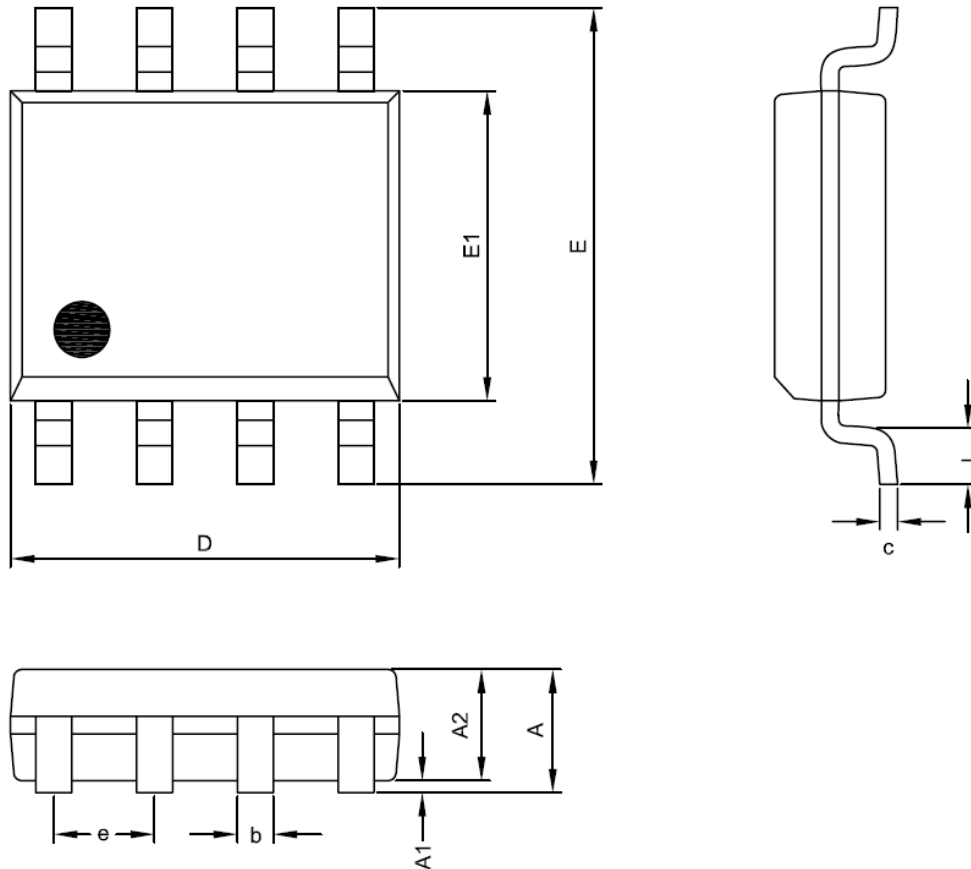


Gate Charge



8. Package Dimensions

SOP8



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes :

1. Jedec outline : MS-012AA
2. Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.