KJ4368P

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Surface-mounted package
- ☑ Super Trench
- ☑ Advanced trench cell design
- ☑ MSL1

1.2 Applications

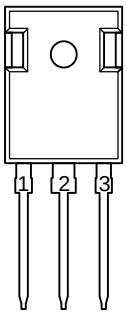
- ☑ BMS appliance
- ☑ Drones
- ☑ High power inverter system
- ☑ Light electric vehicles

1.3 Quick reference

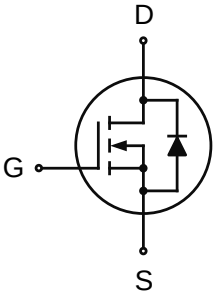
- ☑ BV ≧85V
- ☑ P_{tot} ≦500W
- ☑ I_D ≦300A
- ☑ $R_{DS(ON)}$ ≦ 1.7mΩ@V_{GS} = 10V

2. Pin Description

Pin	Description
1	Gate(G)
2	Drain(D)
3	Source(S)



Top View
TO-247



3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C=25℃	85	-	V
V_{GS}	Gate-Source Voltage	T_C=25℃	-	±20	V
I_D	Drain Current (DC)	T_C=25℃, V_{GS}=10V	-	300	A
I_D	Drain Current (DC)	T_C=100℃, V_{GS}=10V	-	267	A
I_{DM}*	Drain Current (Pulsed)	T_C=25℃, V_{GS}=10V	-	1200	A
P_{tot}	Drain Power Dissipation	T_C=25℃	-	500	W
T_{stg}	Storage Temperature		-55	150	℃
T_J	Junction Temperature		-	150	℃
I_S	Continuous-Source Current	T_C=25℃	-	300	A
E_{AS}	Single Pulsed Avalanche Energy	V_{DD}=40V,L=0.5mH	-	2800	mJ
$R_{\theta JA}$**	Thermal Resistance-Junction to Ambient		-	32.8	℃/W
$R_{\theta JC}$**	Thermal Resistance-Junction to Case		-	0.45	℃/W

Notes:

* Pulse width ≤ 300μs, duty cycle ≤ 2%

** Surface Mounted on minimum footprint pad area

*** Limited by bonding wire

4. Marking Information

Product Name	Marking
KJ4368P	**KJ4368P** **YWWWXX** **YWWWX: Date Code**

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ4368P	**TO-247**	**-**	**-**	**600**	

Note: KUAIJIEXIN defines “Green” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C)

6. Electrical Characteristics (T_A=25℃ Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250μA	85	95	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250μA	2	-	4	V
I_{DSS}	Drain Leakage Current	V_{DS}=80V, V_{GS}=0V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{GS}=0V, V_{GS}=±20V	-	-	±100	nA
$R_{DS(ON)}$ [a]	On-State Resistance	V_{GS}=10V, I_{DS}=50A	-	1.5	1.7	mΩ
Diode Characteristics						
V_{SD} [a]	Diode Forward Voltage	I_{SD}=50A, V_{GS}=0V	-	-	1.2	V
trr	Reverse Recovery Time	I_{DS}=50A, V_{GS}=0V d_{ISD}/dt=100A/μs	-	120	-	ns
Qrr	Reverse Recovery Charge		-	360	-	nC
Dynamic Characteristics [b]						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=50V, Frequency=1MHz	-	14490	-	pF
C_{oss}	Output Capacitance		-	2350	-	
C_{rss}	Reverse Transfer Capacitance		-	472	-	
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=50V, V_{GEN}=10V, R_G=4.5Ω, R_L=1Ω, I_{DS}=50A	-	39	-	ns
t_r	Turn-on Rise Time		-	122	-	
$t_{d(off)}$	Turn-off Delay Time		-	115	-	
t_f	Turn-off Fall Time		-	137	-	
Gate Charge Characteristics [b]						
Q_g	Total Gate Charge	V_{DS}=50V, V_{GS}=10V, I_{DS}=50A	-	240	-	nC
Q_{gs}	Gate-Source Charge		-	56	-	
Q_{gd}	Gate-Drain Charge		-	60	-	

Notes：

a: Pulse test; Pulse width ≤ 300μs, duty cycle ≤ 2%

b: Guaranteed by design, not subject to production testing

7. Typical Characteristics

Figure 1. Maximum Continuous Drain Current vs Case Temperature

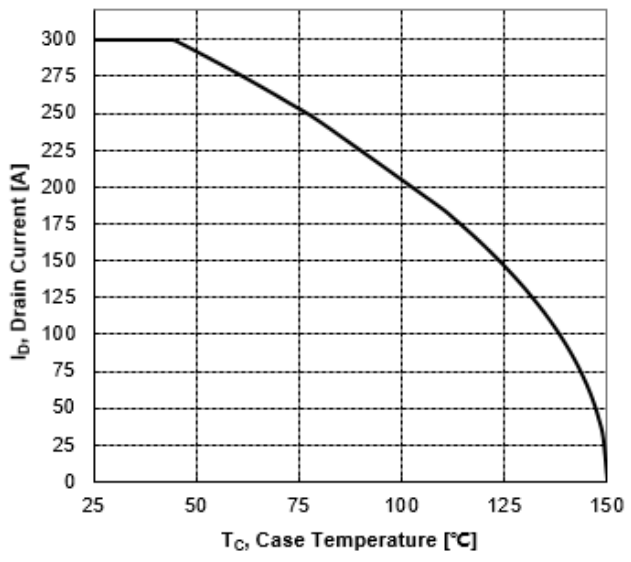


Figure 2. Typical Output Characteristics

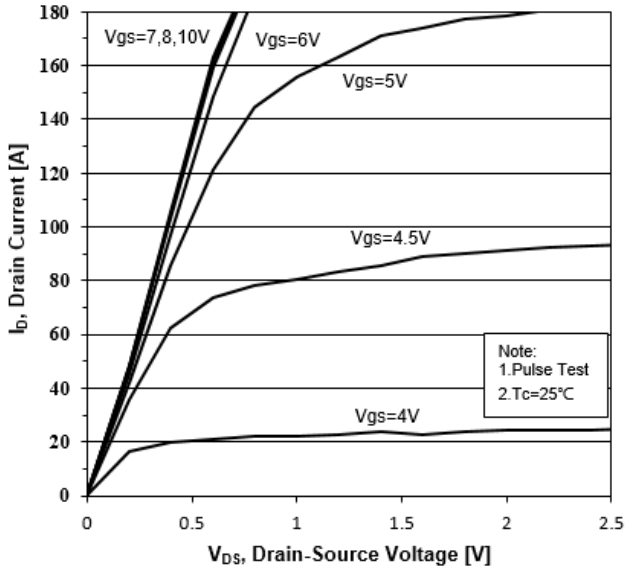


Figure 3. Typical Transfer Characteristics

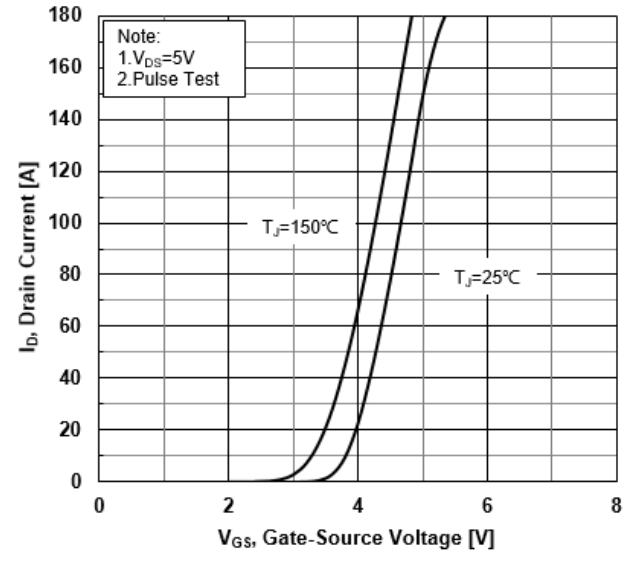
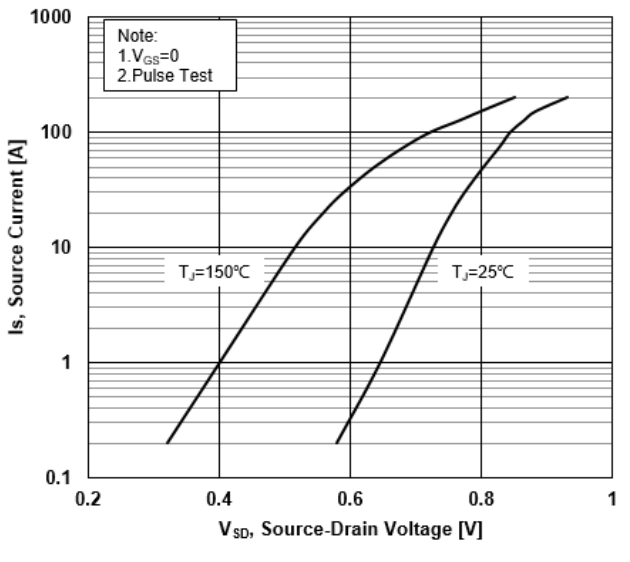


Figure 4. Source-Drain Diode Forward Characteristics



7. Typical Characteristics (cont.)

Figure 5. Drain-Source On-Resistance vs Drain Current

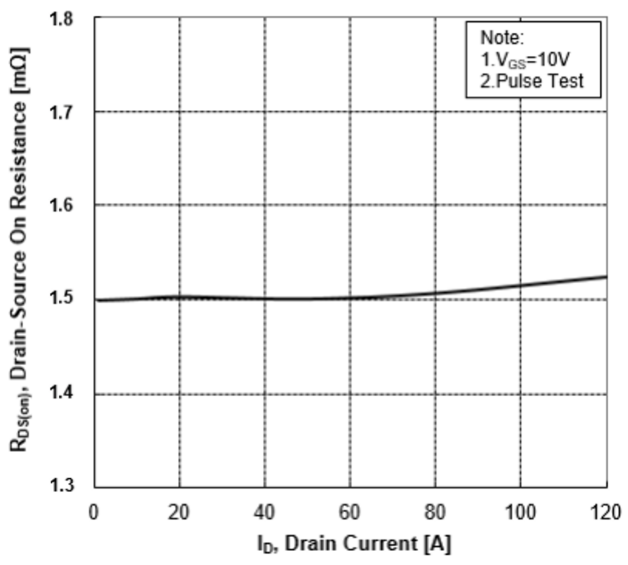


Figure 6. Normalized On-Resistance vs Junction Temperature

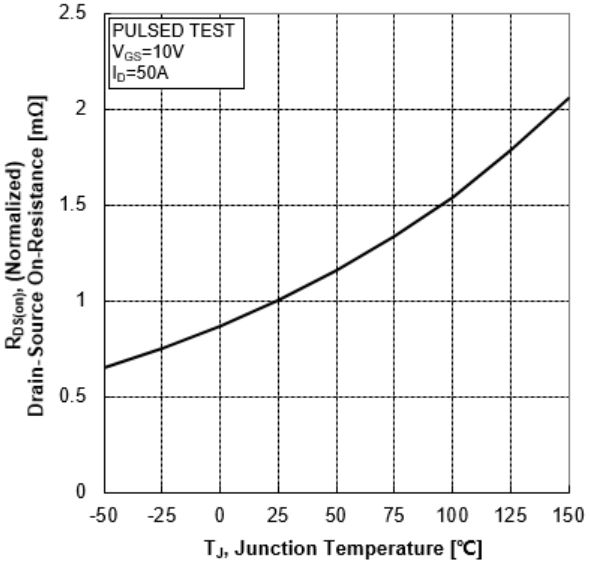


Figure 7. Normalized Threshold Voltage vs Junction Temperature

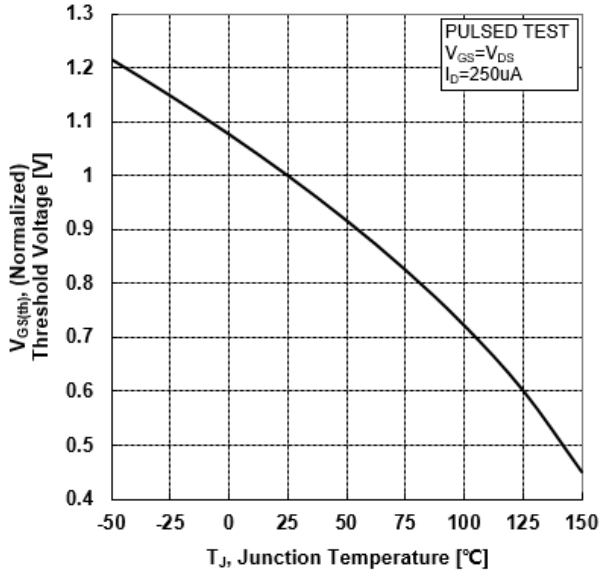
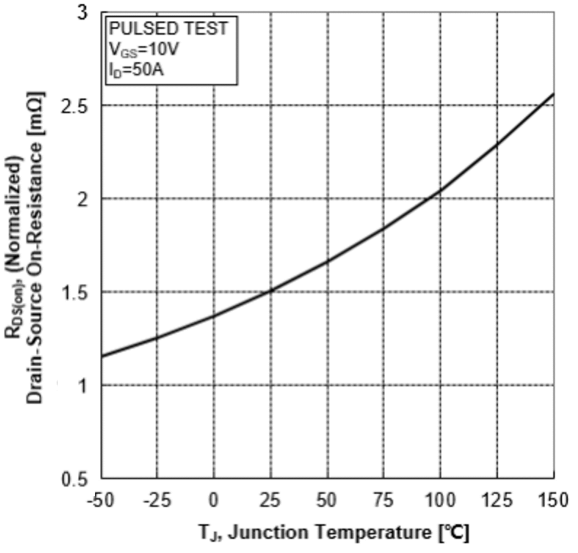


Figure 8. Normalized Breakdown Voltage vs Junction Temperature



7. Typical Characteristics (cont.)

Figure 9. Capacitance Characteristics

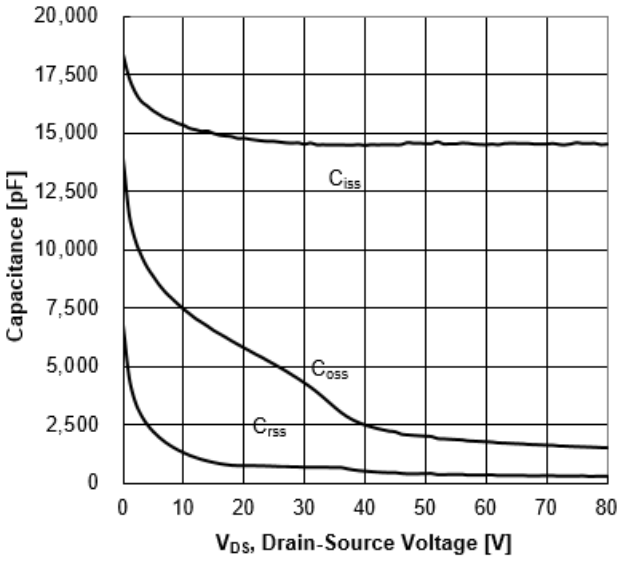
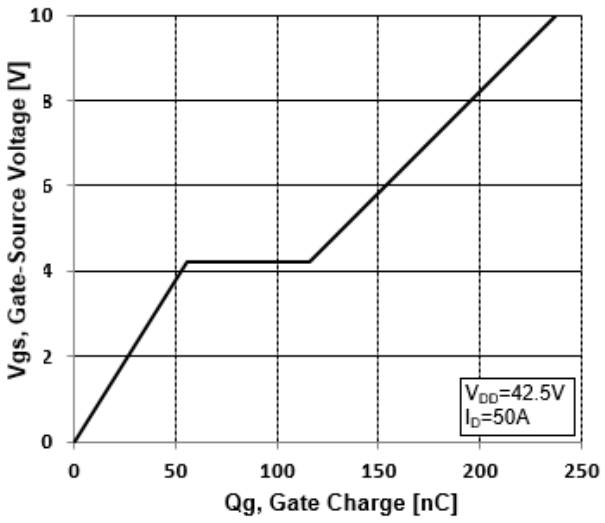


Figure 10. Typical Gate Charge vs Gate-Source Voltage



8. Test Circuit and Waveform

Figure 11. Resistive Switching Test Circuit

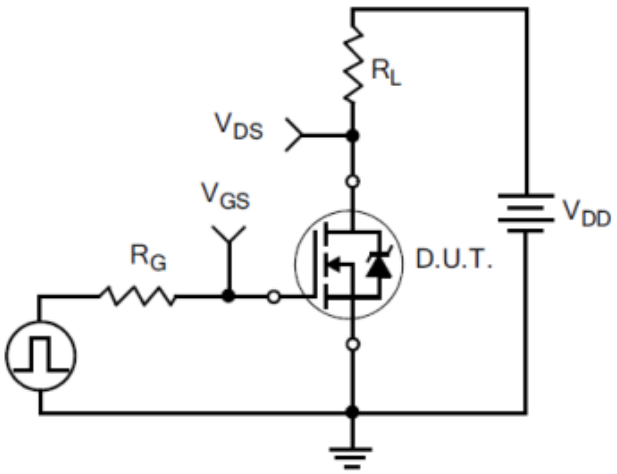
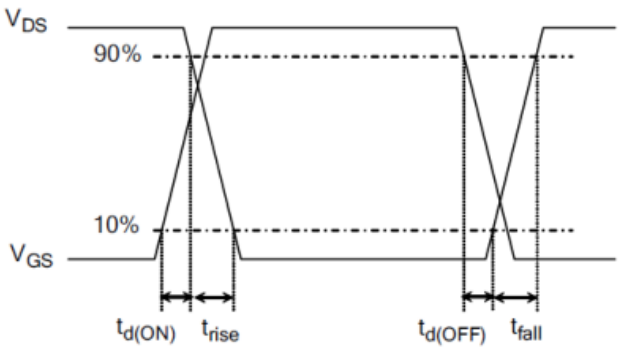


Figure 12. Resistive Switching Waveforms



8. Test Circuit and Waveform (cont.)

Figure 13. Gate Charge Test Circuit	Figure 14. Gate Charge Waveforms

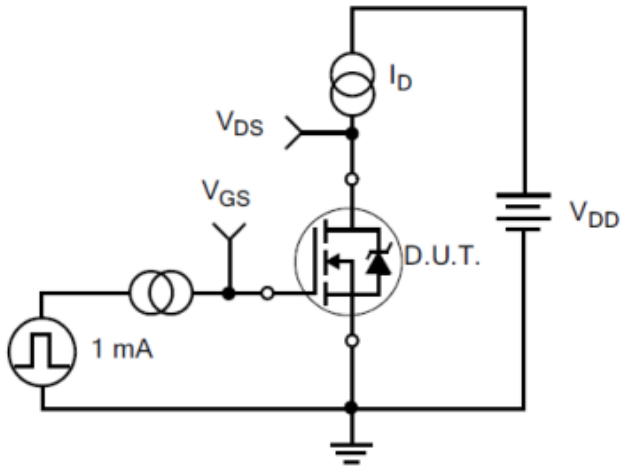
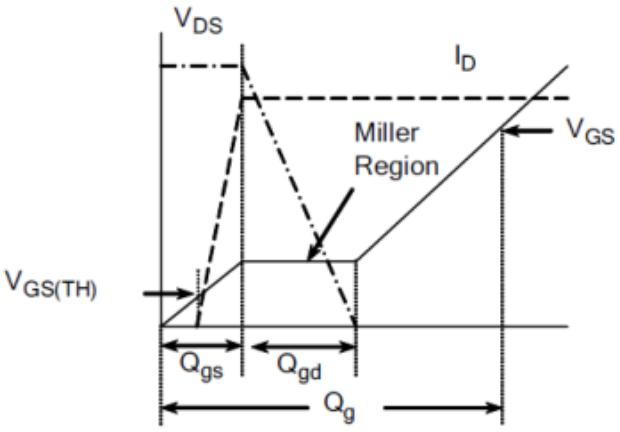
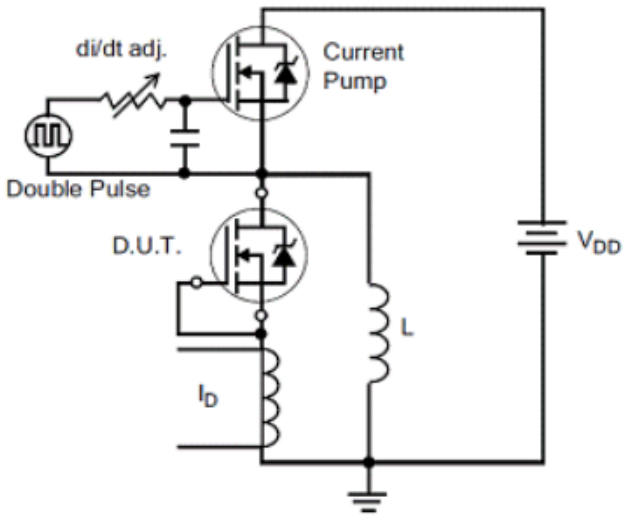
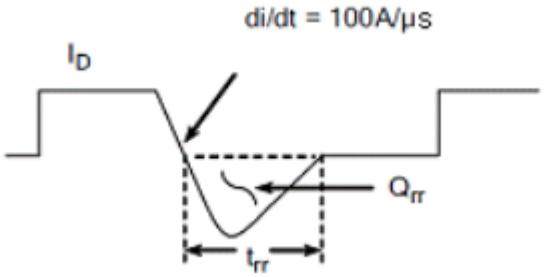
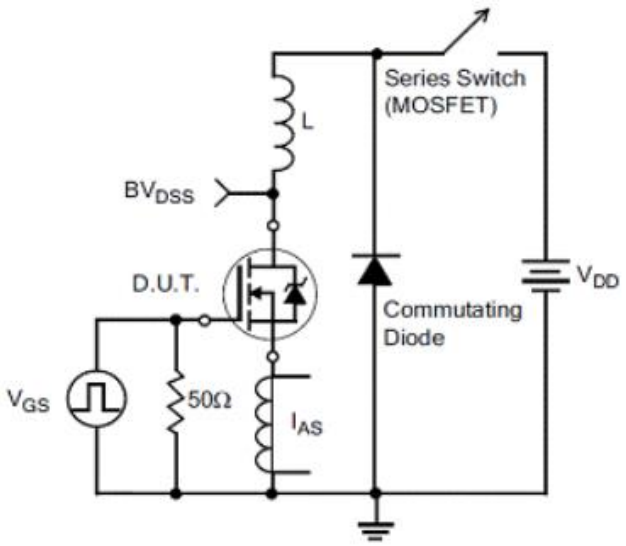
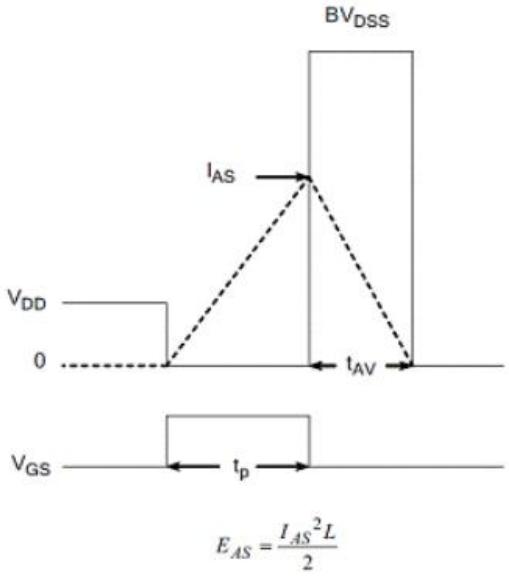

	

Figure 15. Diode Reverse Recovery Test Circuit	**Figure 16. Diode Reverse Recovery Waveform**
	

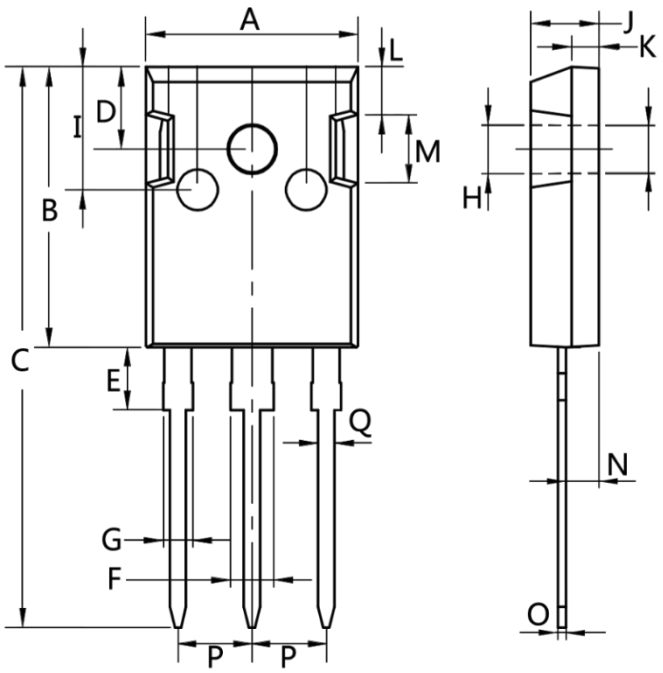
8. Test Circuit and Waveform (cont.)

Figure 17. Unclamped Inductive Switching Test Circuit	Figure 18. Unclamped Inductive Switching Waveform
	

$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

9. Package Dimensions

TO-247 Package



Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3