

P-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Surface-mounted package
- ☑ Advanced trench cell design
- ☑ Extremely low threshold voltage
- ☑ ESD 2KV

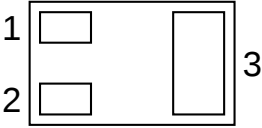
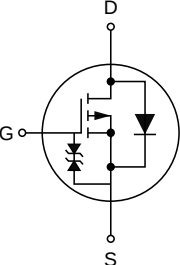
1.2 Applications

- ☑ Portable appliances

1.3 Quick reference

- ☑ $BV \geq -20\text{ V}$
- ☑ $P_{\text{tot}} \leq 0.43\text{ W}$
- ☑ $I_D \leq -0.5\text{ A}$
- ☑ $R_{\text{DS(ON)}} \leq 0.8\ \Omega @ V_{\text{GS}} = -4.5\text{ V}$
- ☑ $R_{\text{DS(ON)}} \leq 1.1\ \Omega @ V_{\text{GS}} = -2.5\text{ V}$
- ☑ $R_{\text{DS(ON)}} \leq 1.5\ \Omega @ V_{\text{GS}} = -1.8\text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate (G)	 Bottom View DFN 1006-3L	
2	Source (S)		
3	Drain (D)		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	Drain-Source Voltage	T _A =25°C	-20	-	V
V _{GS}	Gate-Source Voltage	T _A =25°C	-	±8	V
I _D *	Drain Current	T _A =25°C, V _{GS} =- 4.5 V	-	- 0.5	A
I _{DM} *,**	Pulsed Drain Current	T _A =25°C, V _{GS} =- 4.5 V	-	- 2	A
P _{tot} *	Total Power Dissipation	T _A =25°C	-	0.43	W
T _{stg}	Storage Temperature		-55	150	°C
T _J	Junction Temperature		-	150	°C
I _S	Diode Forward Current	T _A =25°C	-	-0.5	A
R _{θJA} *	Thermal Resistance-Junction to Ambient		-	290	°C/W

Notes :

- * Surface Mounted on 1 in² pad area, t ≤ 10 sec
- ** Pulse width ≤ 300 μs, duty cycle ≤ 2%

4. Marking Information

Product Name	Marking
KJ850P02N1	

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ850P02N1	DFN1006-3			10000	

Note: KUIJIEXIN defines "Green" as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C)

6. Electrical Characteristics (T_A=25°C Unless Otherwise Noted)

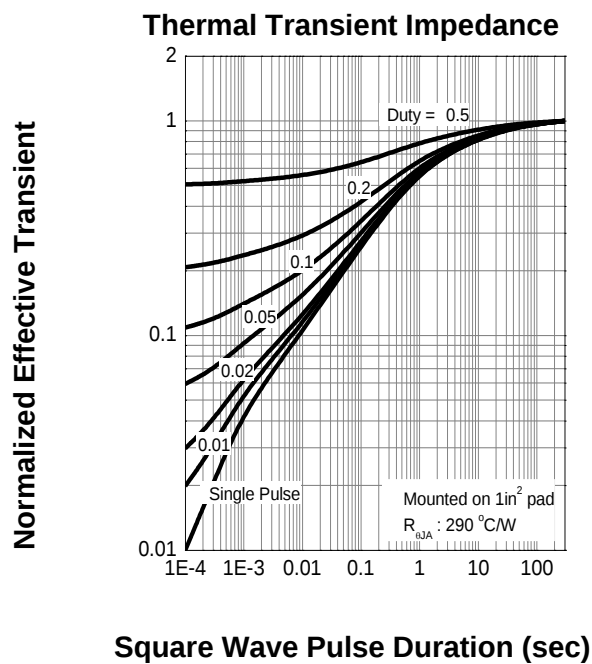
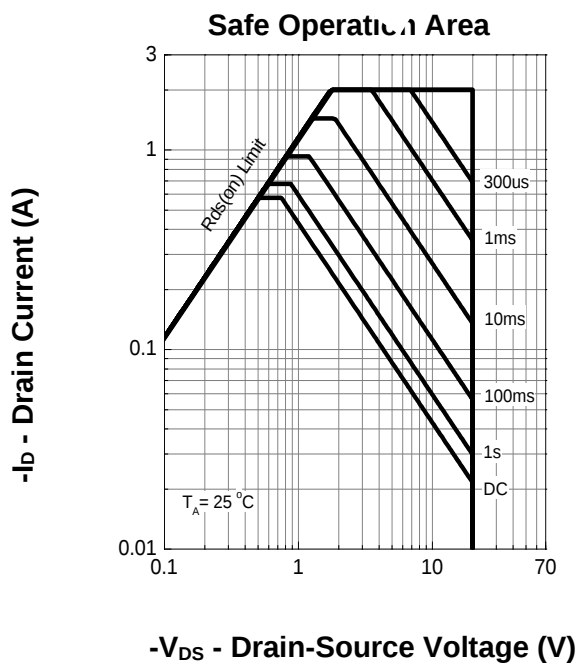
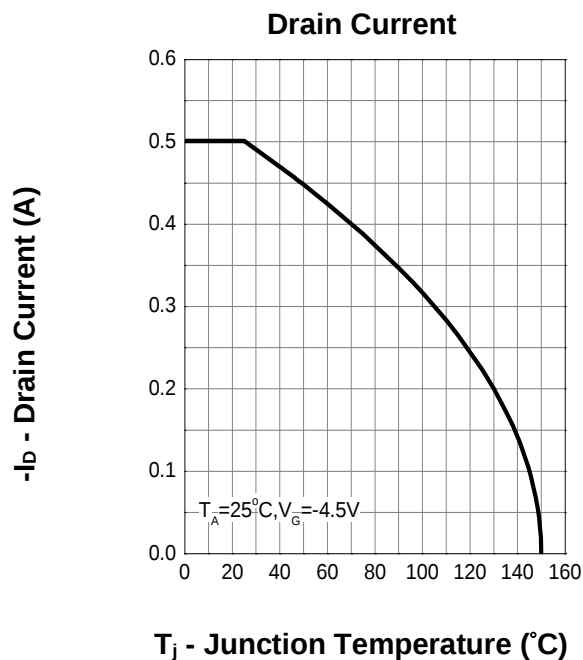
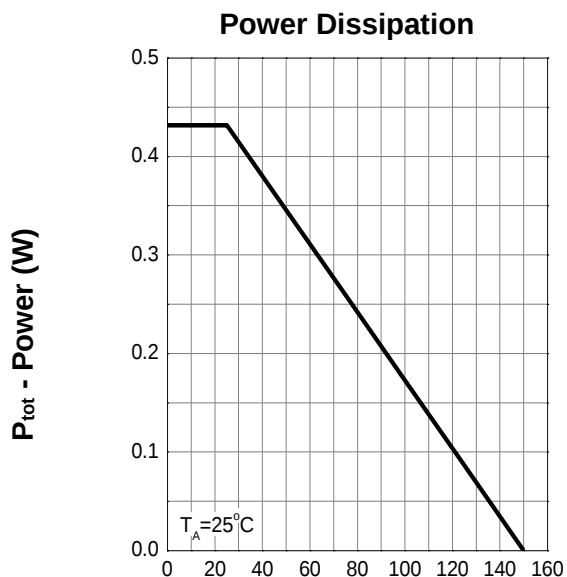
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0 V, I _{DS} =-250 μA	-20	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =-250 μA	-0.5	-	-1	V
I _{DSS}	Drain Leakage Current	V _{DS} =-16 V, V _{GS} =0 V	-	-	-1	μA
		T _J =85°C	-	-	-30	μA
I _{GSS}	Gate Leakage Current	V _{GS} =± 8 V, V _{DS} =0 V	-	-	±10	μA
R _{DS(ON)} ^a	On-State Resistance	V _{GS} =-4.5 V, I _{DS} =-0.5 A	-	0.7	0.8	Ω
		V _{GS} =-2.5 V, I _{DS} =-0.2 A	-	0.9	1.1	
		V _{GS} =-1.8 V, I _{DS} =-0.1 A	-	1.1	1.5	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} =-0.5 A, V _{GS} =0 V	-	-	-1.1	V
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{GS} =0 V, V _{DS} =-10 V Frequency=1 MHz	-	103	-	pF
C _{oss}	Output Capacitance		-	12	-	
C _{rss}	Reverse Transfer Capacitance		-	6.7	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} =-10 V, V _{GEN} =-4.5 V, R _G =4.5 Ω, R _L =20 Ω, I _{DS} =-0.5 A	-	7.5	-	ns
t _r	Turn-on Rise Time		-	22	-	
t _{d(off)}	Turn-off Delay Time		-	189	-	
t _f	Turn-off Fall Time		-	115	-	
Q _g	Total Gate Charge	V _{GS} =-4.5 V, V _{DS} =-10 V, I _{DS} =-0.5 A	-	1.2	-	nC
Q _{gs}	Gate-Source Charge		-	0.4	-	
Q _{gd}	Gate-Drain Charge		-	0.2	-	

Notes :

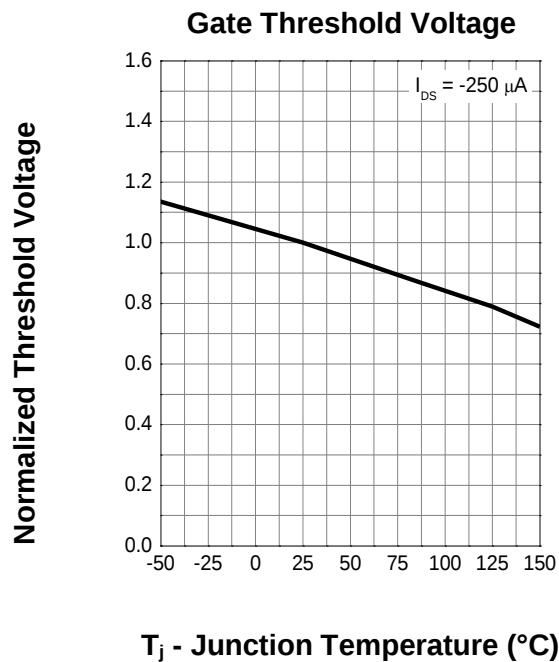
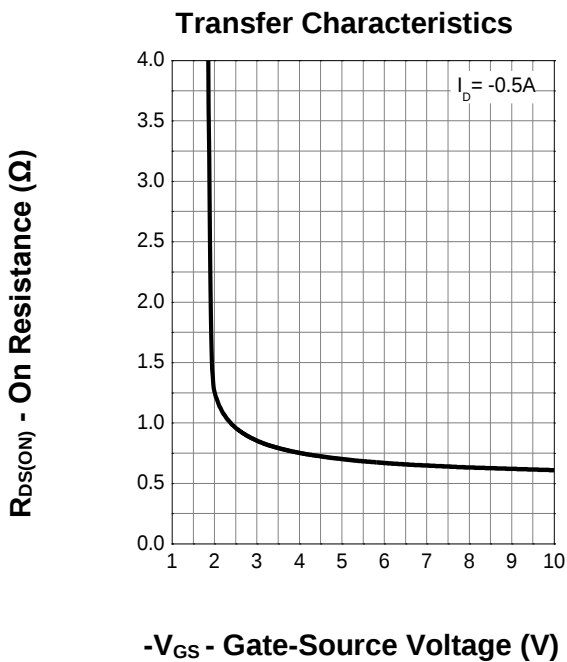
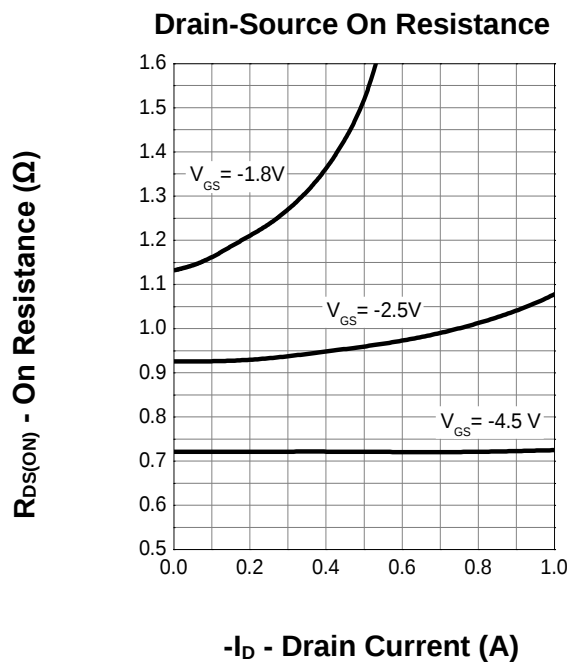
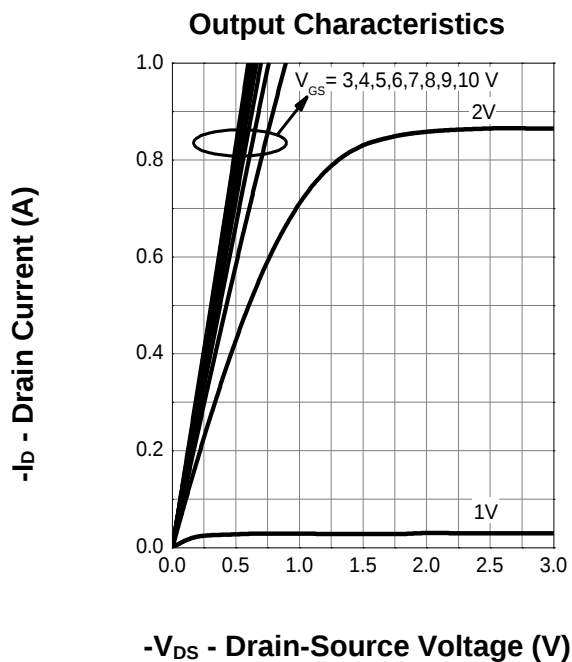
a : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2%

b : Guaranteed by design, not subject to production testing

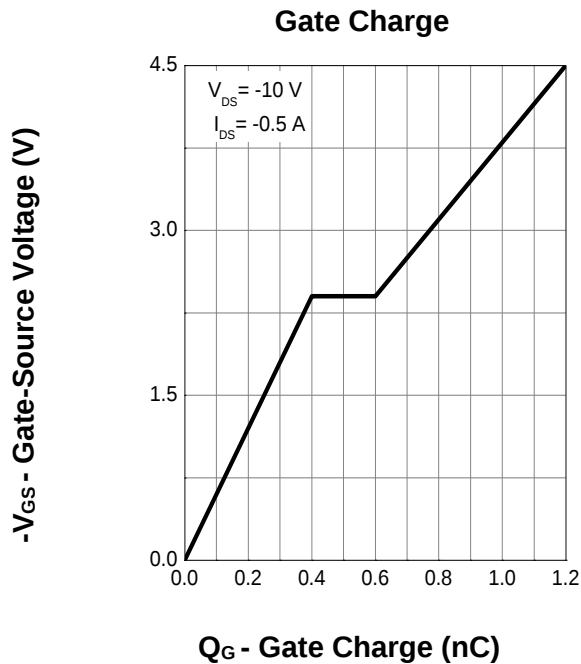
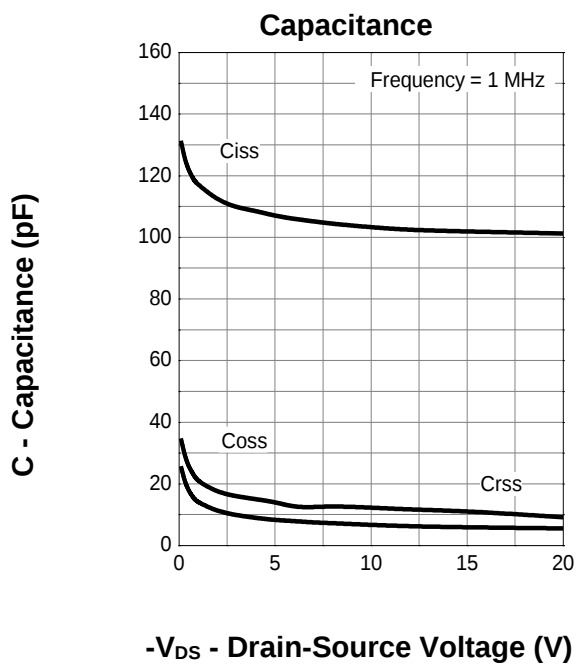
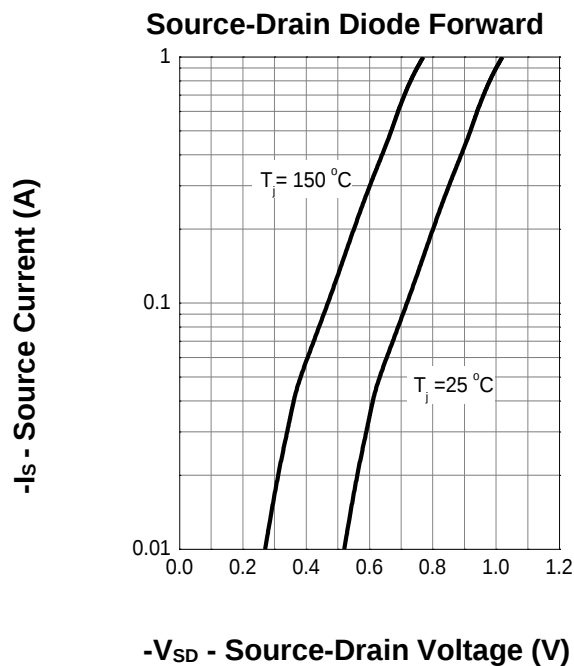
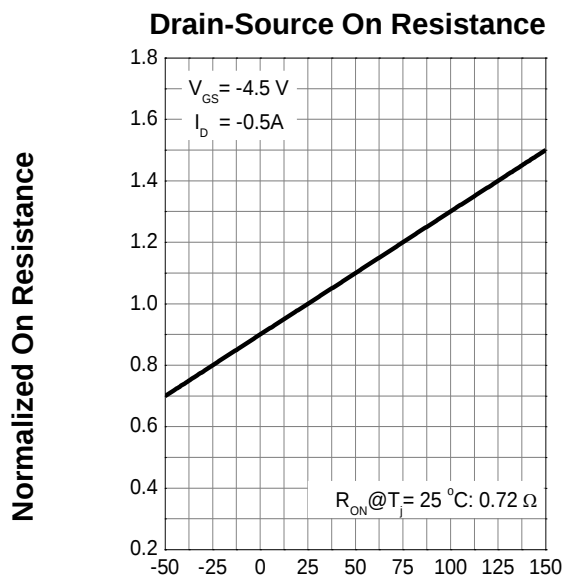
7. Typical Characteristics



7. Typical Characteristics (cont.)

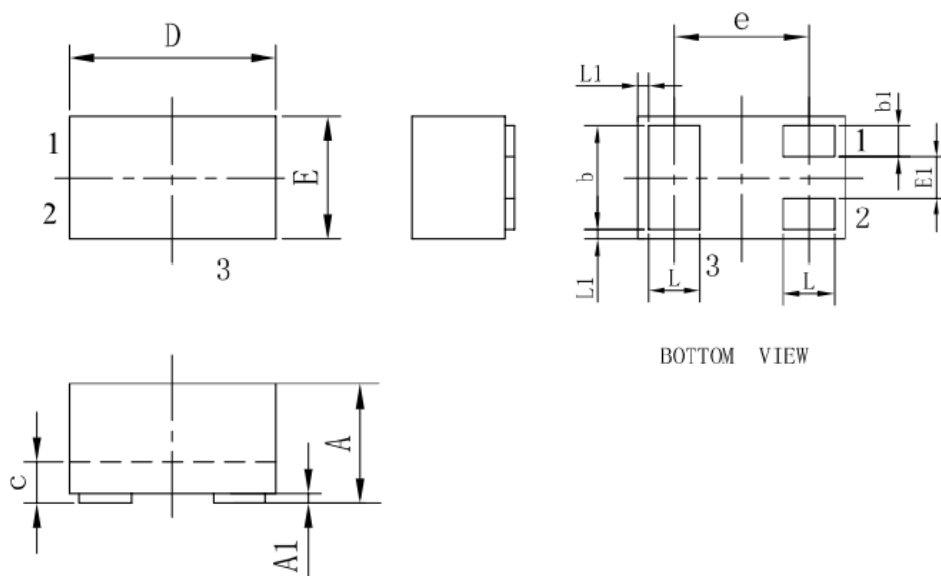


7. Typical Characteristics (cont.)



8. Package Dimensions

DFN1006-3L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0	0.02	0.05
b	0.45	0.50	0.55
b1	0.10	0.15	0.20
c	0.12	0.15	0.18
D	0.95	1.00	1.05
e	0.65BSC		
E	0.55	0.60	0.65
E1	0.15	0.20	0.25
L	0.20	0.25	0.30
L1	0.05REF		