

Dual P-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- Surface-mounted package
- Low gate charge

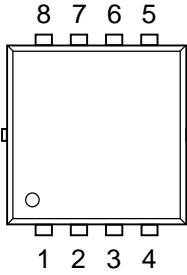
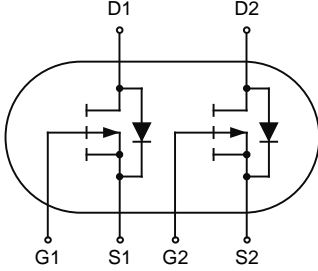
1.2 Applications

- PWM applications
- Load switch

1.3 Quick reference

- $BV \geq -20\text{ V}$
- $R_{DS(ON)} \leq 26\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
- $P_{tot} \leq 40\text{ W}$
- $R_{DS(ON)} \leq 37\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
- $I_D \leq -8\text{ A}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Source(S2)	 <p>Top View PDFN3.3x3.3-8L</p>	
2	Gate(G2)		
3	Source(S1)		
4	Gate(G1)		
5,6	Drain(D1)		
7,8	Drain(D2)		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_A=25^{\circ}\text{C}$	-	-20	V
V_{GS}	Gate-Source Voltage	$T_A=25^{\circ}\text{C}$	-	± 12	V
I_D^*	Drain Current	$T_A=25^{\circ}\text{C}, V_{GS}=-10\text{ V}$	-	-8	A
		$T_A=70^{\circ}\text{C}, V_{GS}=-10\text{ V}$	-	-6.4	A
I_{DM}^{***}	Pulsed Drain Current	$T_A=25^{\circ}\text{C}, V_{GS}=-10\text{ V}$	-	-32	A
P_{tot}	Total Power Dissipation	$T_A=25^{\circ}\text{C}$	-	40	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55	150	$^{\circ}\text{C}$
$R_{\theta JC}^*$	Thermal Resistance-Junction to Case		-	3.15	$^{\circ}\text{C}/\text{W}$

Notes:

- * Surface Mounted on 1 in² pad area, $t \leq 10\text{ sec}$
- ** Pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$
- *** Limited by bonding wire

4. Marking Information

Product Name	Marking
KJ08P02QD	08P02D YWWXXX YWW: Date Code

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ08P02QD	PDFN 3.3×3.3-8L	13 inches	12 mm	5000	

Note: KUIJIEXIN defines "Green" as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C)

6. Electrical Characteristics (T_A=25°C Unless Otherwise Noted)

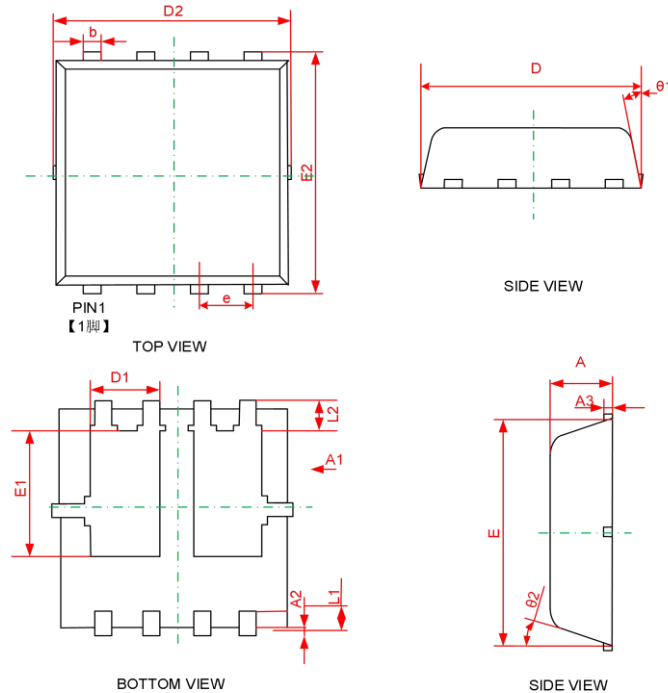
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0 V, I _{DS} =-250 μA	-20	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =-250 μA	-0.45	-0.7	-1.0	V
I _{DSS}	Drain Leakage Current	V _{DS} =-20 V, V _{GS} =0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{GS} =±12 V, V _{DS} =0 V	-	-	±100	nA
R _{DS(ON)} ^a	On-State Resistance	V _{GS} =-4.5 V, I _D =-8 A	-	17	26	mΩ
		V _{GS} =-2.5 V, I _D =-5 A	-	22	37	
g _{fs} ^a	Forward transconductance	V _{GS} =-5 V, I _D =-8 A	-	5	-	S
Dynamic Characteristics^b						
C _{iss}	Input Capacitance	V _{DS} =-10 V, V _{GS} =-5 V, I _D =-5 A, F=1 MHz	-	1205	-	pF
C _{oss}	Output Capacitance		-	194	-	
C _{rss}	Reverse Transfer Capacitance		-	167	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} =-10 V, V _{GS} =-4.5 V, R _L =10 Ω, I _D =-5 A	-	12	-	ns
t _r	Turn-on Rise Time		-	36	-	
t _{d(off)}	Turn-off Delay Time		-	30	-	
t _f	Turn-off Fall Time		-	10	-	
Gate Charge Characteristics^b						
Q _g	Total Gate Charge	V _{DS} =-10 V, V _{GS} =-4.5 V, I _{DS} =-5 A	-	34	-	nC
Q _{gs}	Gate-Source Charge		-	3.5	-	
Q _{gd}	Gate-Drain Charge		-	11	-	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} =-1.25 A, V _{GS} =0 V	-	-	-1.2	V

Notes:

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%
- Guaranteed by design, not subject to production testing

8. Package Dimensions

PDFN 3.3x3.3-8L Package



Symbol	Dimensions in Millimeters	
	Min	Max
A	0.750	0.850
A1	0.000	0.050
A2	0.100	0.200
A3	0.152 REF.	
b	0.200	0.400
D	3.050	3.250
D1	0.935	1.135
D2	3.200	3.400
E	2.900	3.100
E1	1.635	1.835
E2	3.150	3.350
e	0.625	0.675
L1	0.350	0.450
L2	0.365	0.465
$\theta 1$	10°	12°
$\theta 2$	10°	12°