KJ2N7002K

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Surface-mounted package
- ☑ Advanced trench cell design
- ☑ Extremely low threshold voltage
- ☑ ESD protected

1.2 Applications

- ☑ Portable appliances
- ☑ Load switch

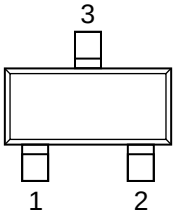
1.3 Quick reference

- ☑ BV ≥ 60 V
- ☑ P_{tot} ≤ 0.83 W
- ☑ I_D ≤ 0.5 A
- ☑ $R_{DS(ON)}$ ≤ 2 mΩ @V_{GS} = 10 V
- ☑ $R_{DS(ON)}$ ≤ 2.7 mΩ @V_{GS} = 4.5 V

2. Pin Description

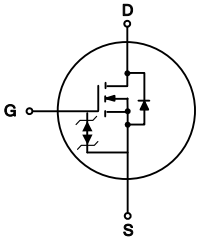
Pin	Description
1	Gate (G)
2	Source (S)
3	Drain (D)

Simplified Outline



Top View
SOT23

Symbol



2. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_A=25℃	60	-	V
V_{GS}	Gate-Source Voltage	T_A=25℃	-	±20	V
I_D *	Drain Current	T_A=25℃, V_{GS}=10 V	-	0.5	A
I_{DM} *, **	Pulsed Drain Current	T_A=25℃, V_{GS}=10 V	-	2	A
P_{tot} *	Total Power Dissipation	T_A=25℃	-	0.83	W
I_S *	Diode Forward Current	T_A=25℃	-	0.5	A
T_J, T_{stg}	Operating junction and storage temperature range		-55	150	℃
$R_{\theta JA}$ *	Thermal Resistance-Junction to Ambient		-	150	℃/W

Notes:

* Surface mounted on 1 in^2 pad area, $t \leq 10$ sec.

** Pulse width ≤ 300 μs, duty cycle ≤ 2%.

*** Limited by bonding wire.

4. Marking Information

Product Name	Marking
KJ2N7002K	**72K**

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ2N7002K	**SOT23**	**7"**	**8 mm**	**3000**	

Note: KUAIJIEXIN defines “Green” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C)

6. Electrical Characteristics (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0 V, I_{DS}=250 μA	60	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250 μA	1	1.5	2	V
I_{DSS}	Drain Leakage Current	V_{DS}=48 V, V_{GS}=0 V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{DS}=0 V, V_{GS}=±20 V	-	±0.8	-	μA
$R_{DS(ON)}$ [a]	On-State Resistance	V_{GS}=10 V, I_{DS}=0.5 A	-	1.5	2	Ω
		V_{GS}=4.5 V, I_{DS}=0.2 A	-	2.0	2.7	
Diode Characteristics						
V_{SD} [a]	Diode Forward Voltage	V_{GS}=0 V, I_{SD}=0.5 A	-	0.85	-	V
t_{rr}	Reverse Recovery Time	I_{SD}=0.5 A, dI_{SD}/dt=100 A/μs	-	30	-	ns
Q_{rr}	Reverse Recovery Charge		-	29	-	nC
Dynamic Characteristics [b]						
R_G	Gate Resistance	V_{GS}=V_{DS}=0V, f=1MHz	-	200	-	Ω
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, Frequency=1MHz	-	14.7	-	pF
C_{oss}	Output Capacitance		-	0.76	-	
C_{rss}	Reverse Transfer Capacitance		-	0.63	-	
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=30 V, V_{GEN}=10 V, R_G=25 Ω, R_L=60 Ω, I_{DS}=0.5 A	-	2.7	-	ns
t_r	Turn-on Rise Time		-	2.5	-	
$t_{d(off)}$	Turn-off Delay Time		-	13	-	
t_f	Turn-off Fall Time		-	8	-	
Gate Charge Characteristics [b]						
Q_g	Total Gate Charge	V_{DS}=10 V, V_{GS}=4.5 V, I_{DS}=0.5 A	-	0.44	-	nC
Q_{gs}	Gate-Source Charge		-	0.2	-	
Q_{gd}	Gate-Drain Charge		-	0.1	-	

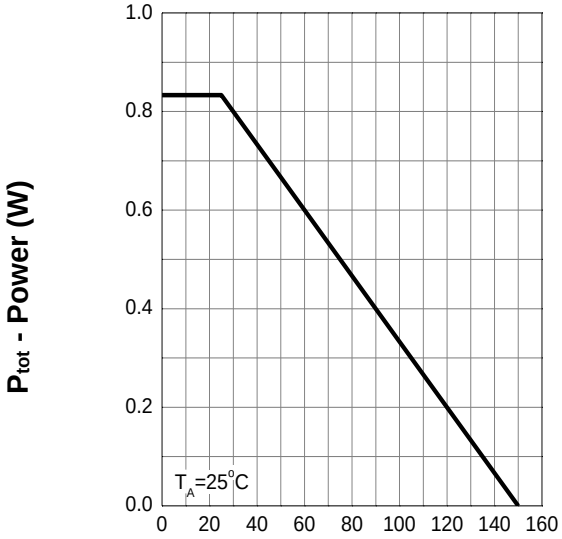
Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

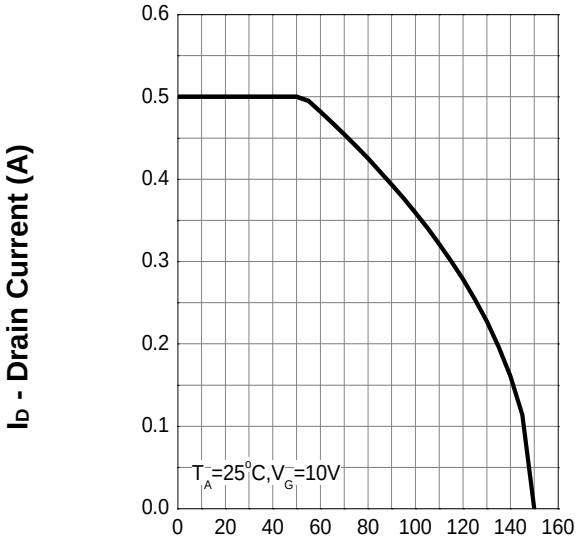
b. Guaranteed by design, not subject to production testing.

7. Typical Characteristics

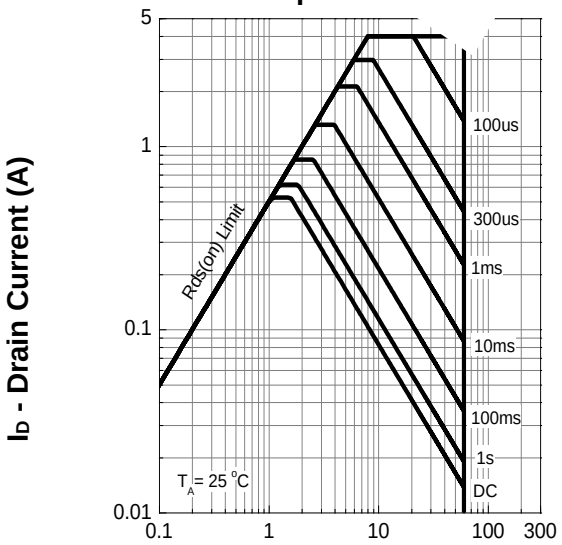
Power Dissipation



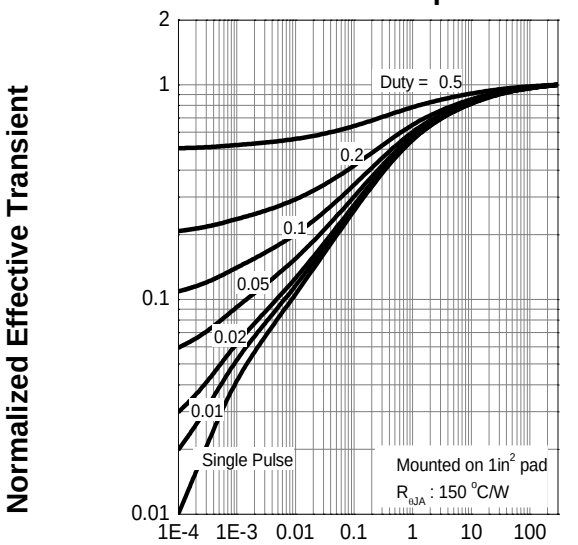
Drain Current



Safe Operatio

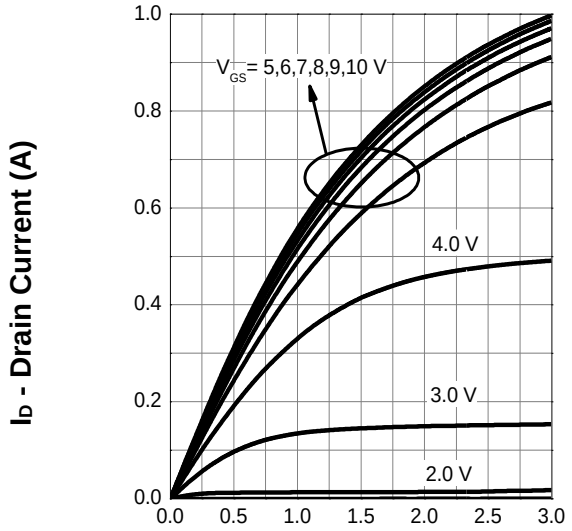


Thermal Transient Impedance

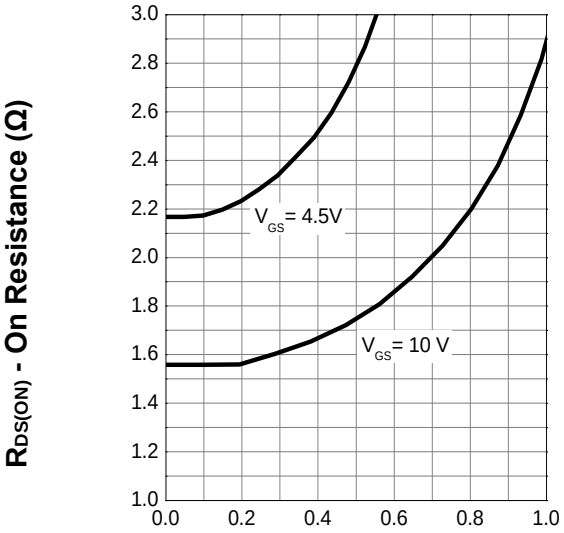


7. Typical Characteristics (cont.)

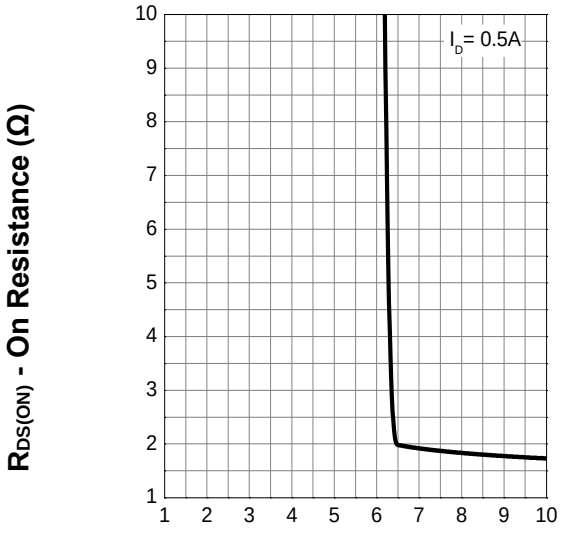
Output Characteristics



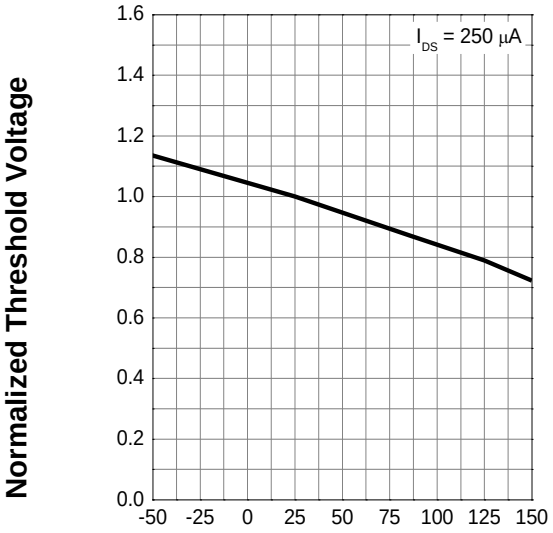
Drain-Source On Resistance



Transfer Characteristics

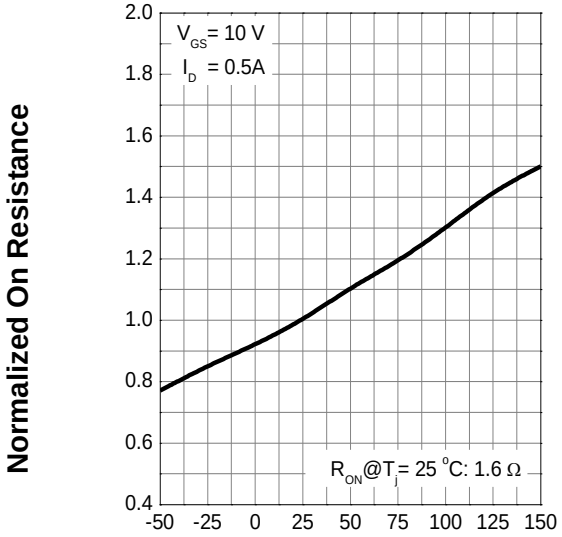


Gate Threshold Voltage

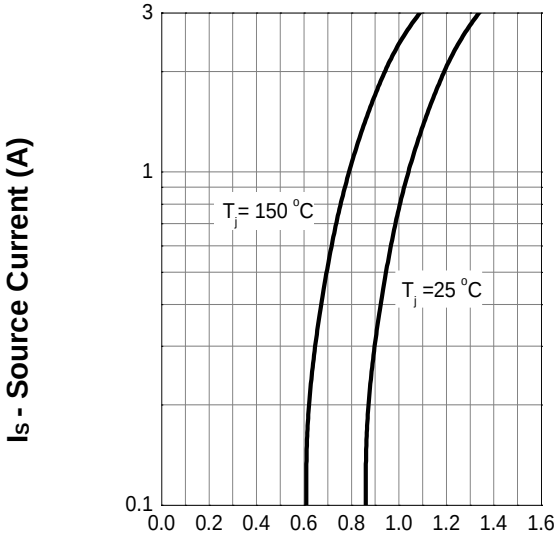


7. Typical Characteristics (cont.)

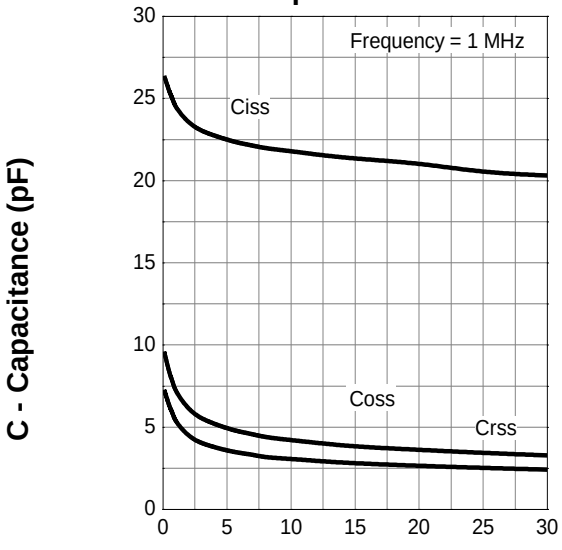
Drain-Source On Resistance



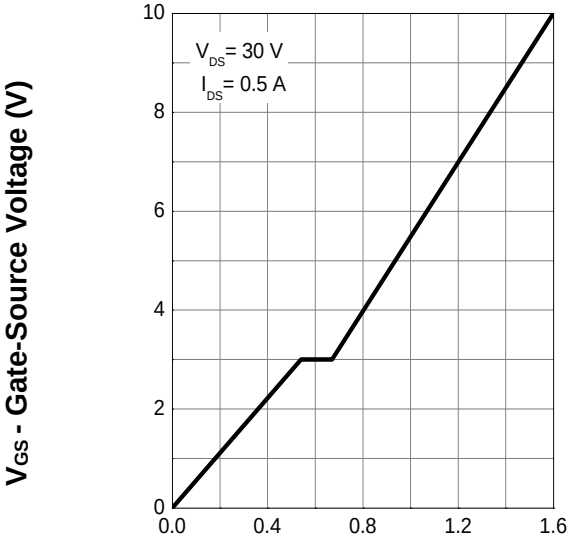
Source-Drain Diode Forward



Capacitance

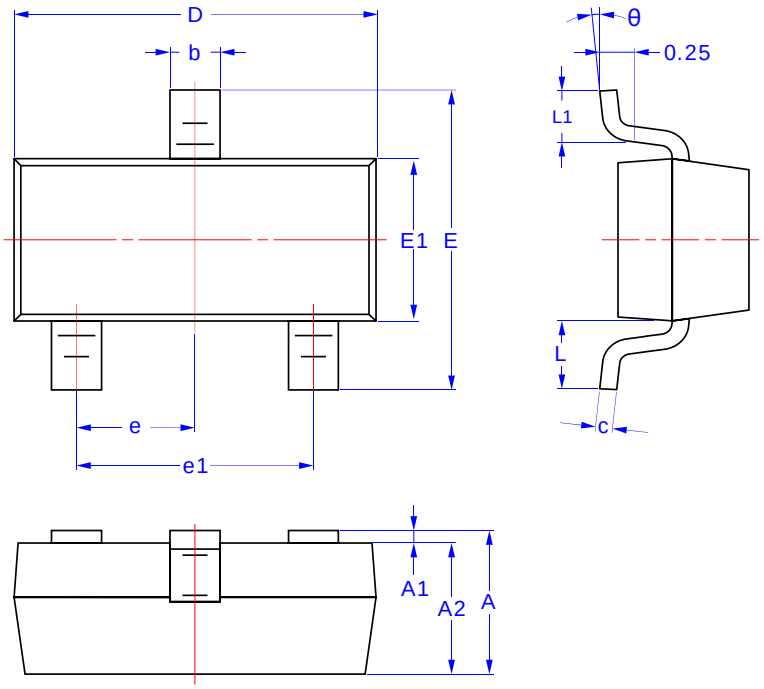


Gate Charge



8. Package Dimensions

SOT23 Package



Symbol	Dimensions in Millimeters	
	Min.	Max.
A	0.90	1.15
A1	0.00	0.10
A2	0.90	1.05
b	0.30	0.50
c	0.08	0.15
D	2.80	3.00
E	2.25	2.55
E1	1.20	1.40
e	0.95 TYP.	
e1	1.80	2.00
L	0.30	0.50
L1	0.55 REF.	
θ	0°	8°