

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☒ Surface-mounted package
- ☒ Advanced trench cell design
- ☒ T_J max 175°C
- ☒ MSL1

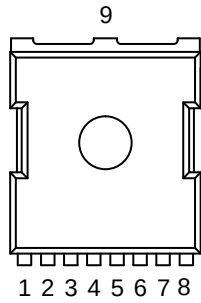
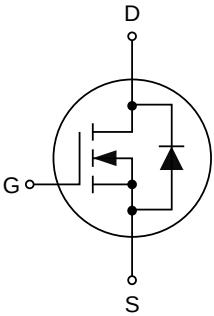
1.2 Applications

- ☒ Power management switches
- ☒ DC/DC converter
- ☒ LED backlighting

1.3 Quick reference

- ☒ $BV \geq 80\text{ V}$
- ☒ $P_D \leq 465\text{ W}$
- ☒ $I_D \leq 400\text{ A}$
- ☒ $R_{DS(ON)} \leq 1.2\text{ m}\Omega @ V_{GS} = 10\text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate	 Top View TOLL-8L	
2,3,4,5,6,7,8	Source		
9	Drain		

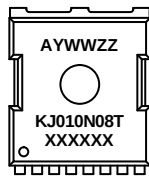
3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_C=25^{\circ}\text{C}$	-	80	V
V_{GS}	Gate-Source Voltage	$T_C=25^{\circ}\text{C}$	-	± 20	V
$I_D^{*,***}$	Drain Current	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	400	A
		$T_C=100^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	250	A
$I_{DM}^{*,**}$	Drain Current (Pulsed)	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	1600	A
P_D	Drain Power Dissipation	$T_C=25^{\circ}\text{C}$	-	465	W
E_{AS}	Single Pulsed Avalanche Energy	$V_{DD}=25\text{ V}, L=0.4\text{ mH}$	-	1280	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55	175	$^{\circ}\text{C}$
$R_{\theta JA}^{**}$	Thermal Resistance-Junction to Ambient		-	40	$^{\circ}\text{C/W}$
$R_{\theta JC}^{**}$	Thermal Resistance-Junction to Case		-	0.32	

Notes:

- * Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- ** Surface mounted on 1 in^2 pad area, $t \leq 10\text{ sec}$.
- *** Limited by bonding wire.

4. Marking Information

Product Name	Marking
KJ010N08T	

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity (pcs)
KJ010N08T	TOLL-8L	13"	24 mm	2000

Note: KUAJIEXIN defines "Green" as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C).

6. Electrical Characteristics (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0 V, I _{DS} =250 μA	80	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250 μA	2	-	4	V
I _{DSS}	Drain Gate Current	V _{DS} =80 V, V _{GS} =0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{DS} =0 V, V _{GS} =±20 V	-	-	±100	nA
R _{DS(ON)} ^a	Drain-Source On-State Resistance	V _{GS} =10 V, I _{DS} =20 A	-	1.0	1.2	mΩ
g _{fs} ^a	Forward Transconductance	V _{GS} =10 V, I _{DS} =20 A	-	62	-	S
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	V _{GS} =0 V, I _{SD} =20 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} =0 V, I _{SD} =20 A, dI _{SD} /dt=100 A/μs	-	128	-	ns
Q _{rr}	Reverse Recovery Charge		-	141	-	nC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{DS} =40 V, V _{GS} =0 V, Frequency=1 MHz	-	13090	-	pF
C _{oss}	Output Capacitance		-	2620	-	
C _{rss}	Reverse Transfer Capacitance		-	120	-	
R _g	Gate Resistance		-	3.1	-	Ω
t _{d(on)}	Turn-on Delay Time	V _{DS} =40 V, V _{GEN} =10 V, R _G =3 Ω, I _{DS} =20 A	-	45	-	ns
t _r	Turn-on Rise Time		-	88	-	
t _{d(off)}	Turn-off Delay Time		-	164	-	
t _f	Turn-off Fall Time		-	95	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} =40 V, V _{GS} =10 V, I _{DS} =30 A	-	245	-	nC
Q _{gs}	Gate-Source Charge		-	64	-	
Q _{gd}	Gate-Drain Charge		-	59	-	

Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

7. Typical Characteristics

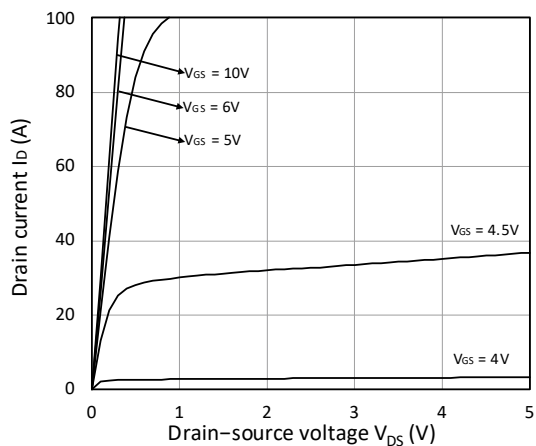


Figure 1. Output Characteristics

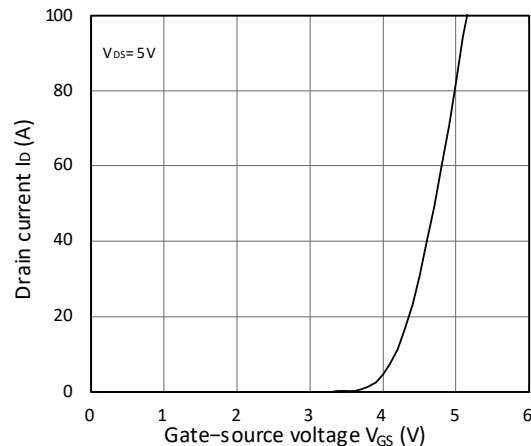


Figure 2. Transfer Characteristics

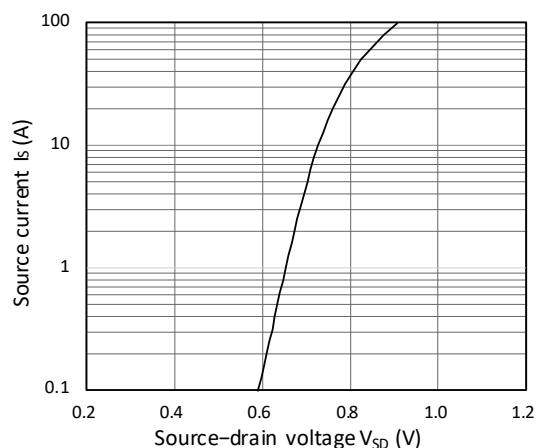


Figure 3. Forward Characteristics of Reverse

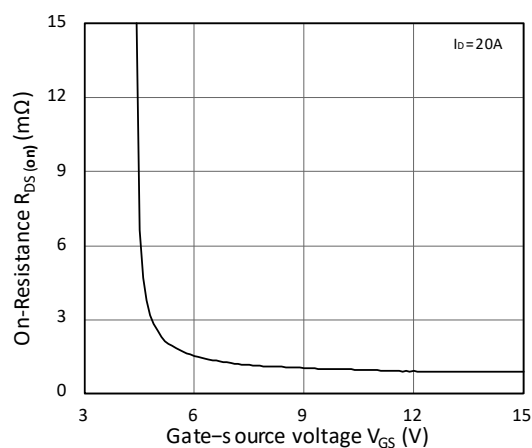


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

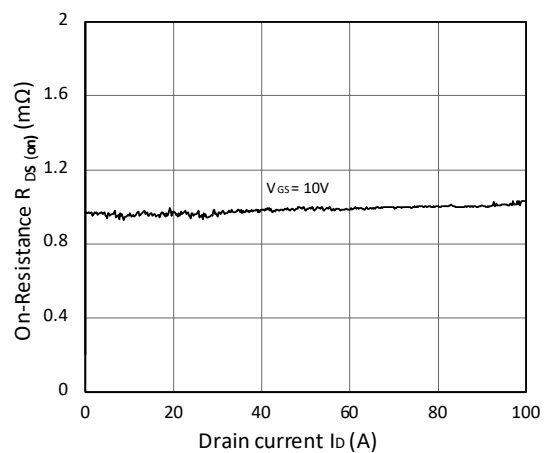


Figure 5. $R_{DS(ON)}$ vs. I_D

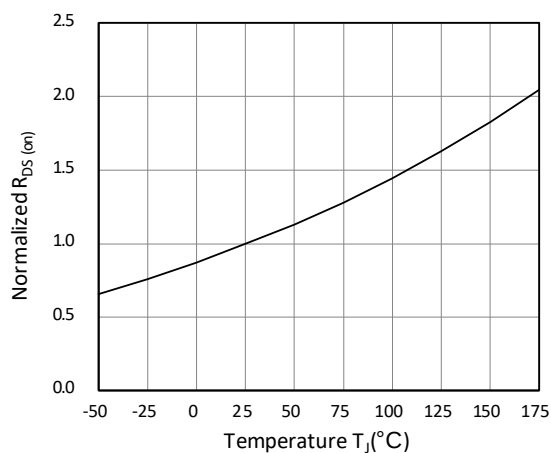


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

7. Typical Characteristics (cont.)

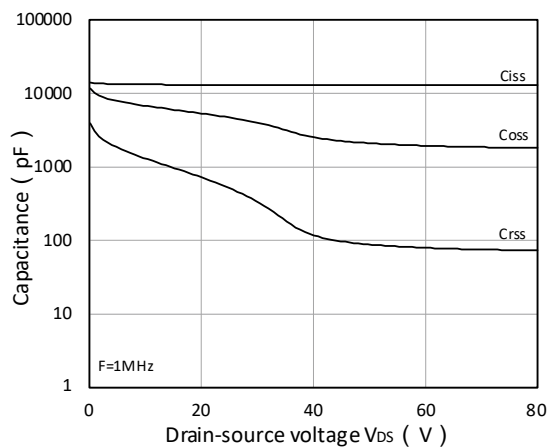


Figure 7. Capacitance Characteristics

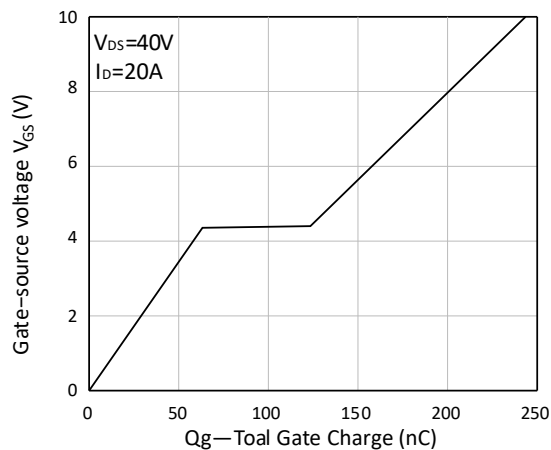


Figure 8. Gate Charge Characteristics

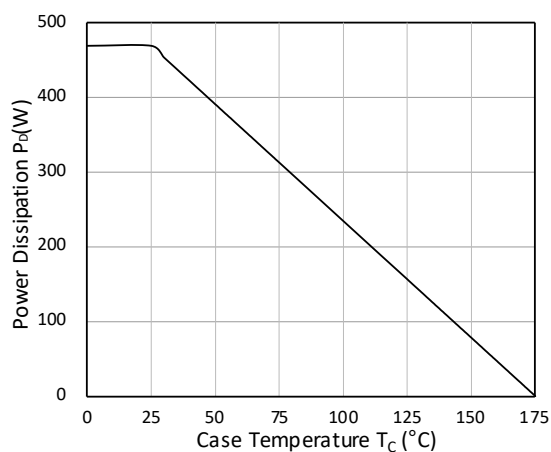


Figure 9. Power Dissipation

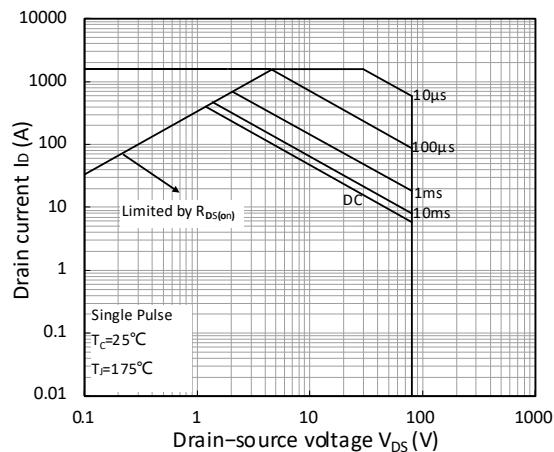


Figure 10. Safe Operating Area

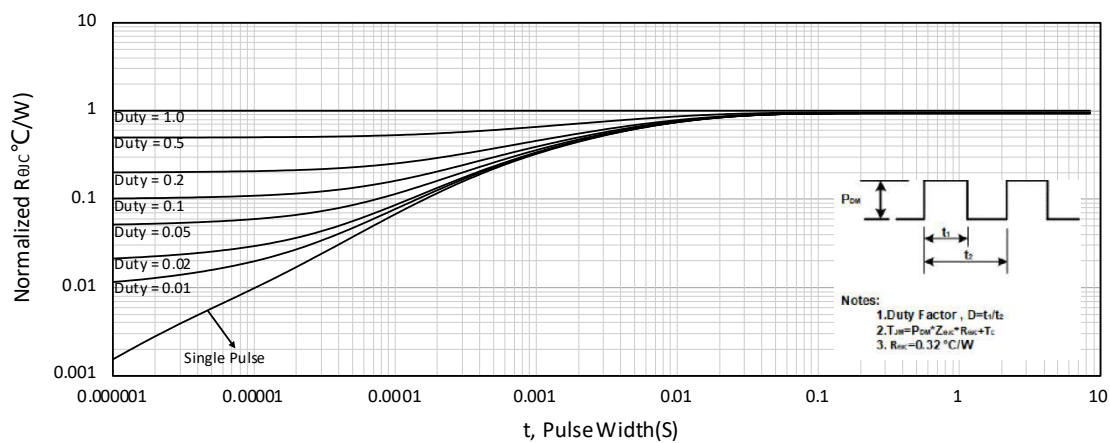


Figure 11. Normalized Maximum Transient Thermal Impedance

7. Test Circuit

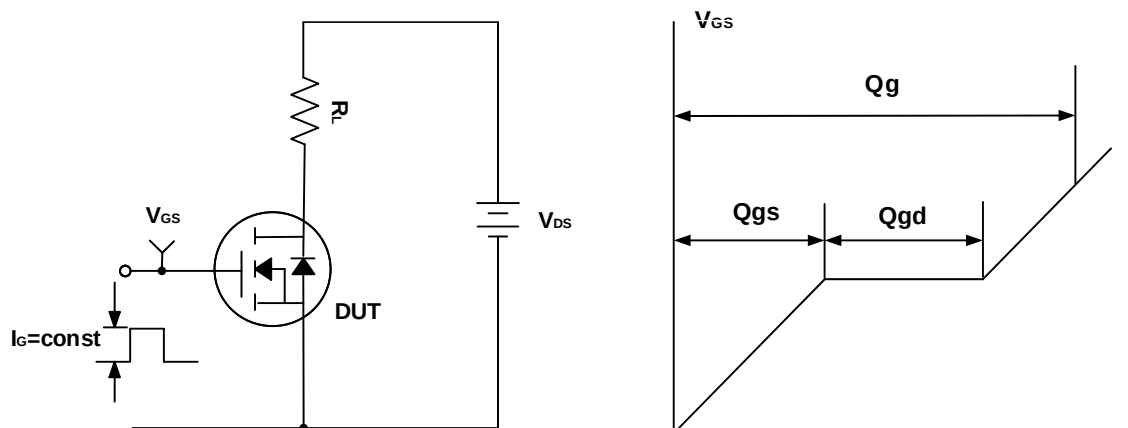


Figure A. Gate Charge Test Circuit & Waveforms

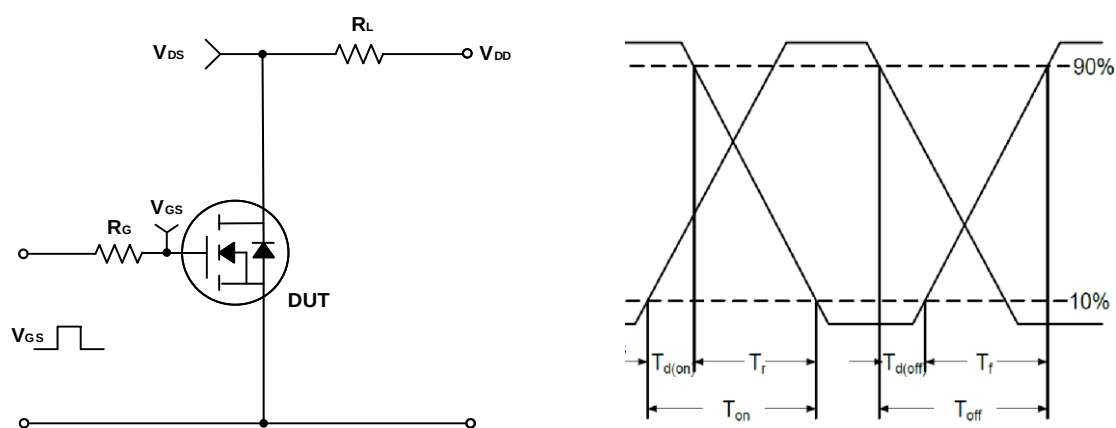


Figure B. Switching Test Circuit & Waveforms

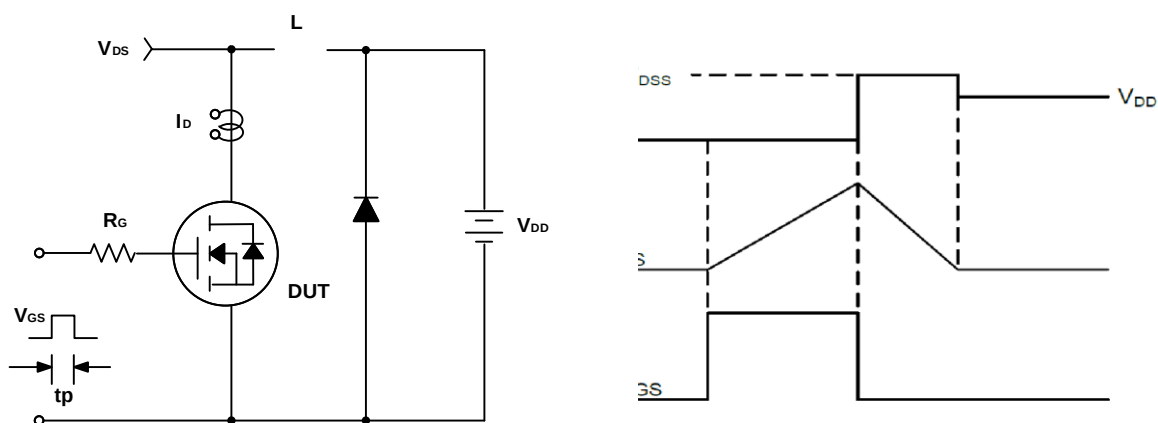
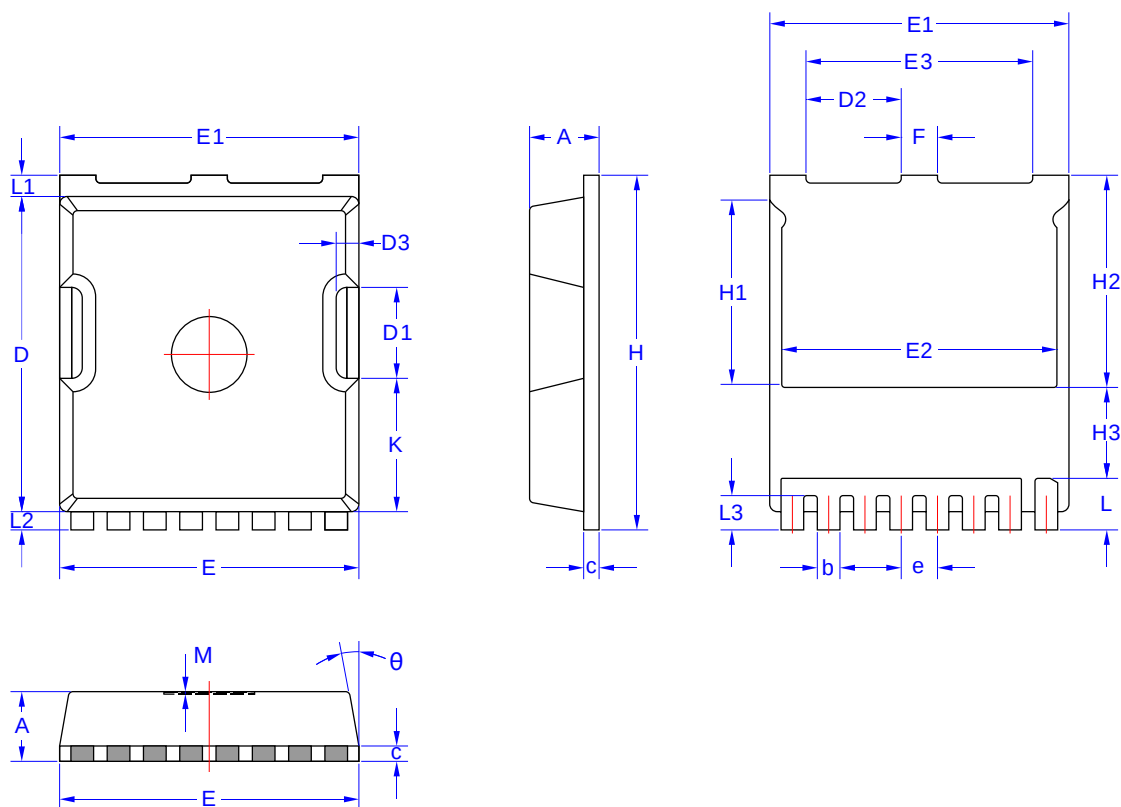


Figure C. Unclamped Inductive Switching Circuit & Waveforms

8. Package Dimensions

TOLL-8L Package



Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
A	2.20	2.30	2.40
b	0.65	0.75	0.85
c		0.508 REF	
D	10.25	10.40	10.55
D1	2.85	3.00	3.15
D2	2.95	3.10	3.25
D3		0.75 REF	
E	9.75	9.90	10.05
E1	9.65	9.80	9.95
E2	8.95	9.10	9.25
E3	7.25	7.40	7.55
e		1.20 BSC	

Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
F	1.05	1.20	1.35
H	11.55	11.70	11.85
H1	6.03	6.18	6.33
H2	6.85	7.00	7.15
H3		3.00 BSC	
K	4.25	4.40	4.55
L	1.55	1.70	1.85
L1	0.55	0.70	0.85
L2	0.45	0.60	0.75
L3	1.00	1.15	1.30
M		0.08 REF	
θ	8°	10°	12°