KJ02N08T

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Surface-mounted package
- ☑ Advanced trench cell design
- ☑ Super Trench
- ☑ MSL1
- ☑ T_J max 175℃

1.2 Applications

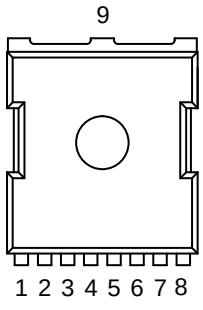
- ☑ BMS appliances
- ☑ High power inverter system
- ☑ Drones
- ☑ Light electric vehicles

1.3 Quick reference

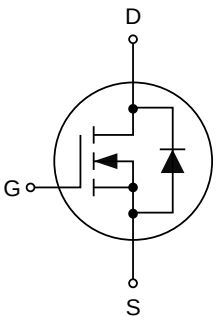
- ☑ BV ≥ 95 V
- ☑ $R_{DS(ON)}$ ≤ 2.8 mΩ @V_{GS} = 10 V
- ☑ P_{tot} ≤ 333 W
- ☑ I_D ≤ 220 A

2. Pin Description

Pin	Description
1	Gate
2,3,4,5,6,7,8	Source
9	Drain



Top View
TOLL-8L



3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C=25℃	95	-	V
V_{GS}	Gate-Source Voltage	T_C=25℃	-	±20	V
I_D ***	Drain Current (DC)	T_C=25℃, V_{GS}=10 V	-	220	A
		T_C=100℃, V_{GS}=10 V	-	156	A
I_{DM} *, ***	Drain Current (Pulsed)	T_C=25℃, V_{GS}=10 V	-	800	A
P_{tot}	Drain Power Dissipation	T_C=25℃	-	333	W
I_S	Continuous-Source Current	T_C=25℃	-	220	A
E_{AS}	Single Pulsed Avalanche Energy	V_{DD}=100 V, L=0.1 mH	-	805	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55	175	℃
$R_{\theta JA}$ **	Thermal Resistance-Junction to Ambient		-	32.8	℃/W
$R_{\theta JC}$ **	Thermal Resistance-Junction to Case		-	0.45	℃/W

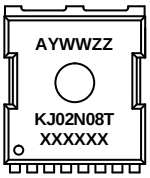
Notes:

* Pulse width ≤ 300 μs, duty cycle ≤ 2%.

** Surface mounted on minimum footprint pad area.

*** Limited by bonding wire.

4. Marking Information

Product Name	Marking
KJ02N08T	

5. Ordering Code

Product Name	Package	Reel size	Tape width	Quantity (pcs)
KJ02N08T	**TOLL-8L**	**13"**	**24 mm**	**2000**

Note: KUAIJIEXIN defines “Green” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C)

6. Electrical Characteristics (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0 V, I_{DS}=250 μA	95	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250 μA	2	-	4	V
I_{DSS}	Drain Leakage Current	V_{DS}=85 V, V_{GS}=0 V	-	-	1	μA
		T_J=85℃	-	-	30	μA
I_{GSS}	Gate Leakage Current	V_{DS}=0 V, V_{GS}=±20 V	-	-	±100	nA
$R_{DS(ON)}$ [a]	On-State Resistance	V_{GS}=10 V, I_{DS}=30 A	-	2.4	2.8	mΩ
Diode Characteristics						
V_{SD} [a]	Diode Forward Voltage	V_{GS}=0 V, I_{SD}=30 A	-	-	1.2	V
trr	Reverse Recovery Time	V_{GS}=0V, I_{DS}=30 A, d_{ISD}/dt=100 A/μs	-	78	-	ns
Qrr	Reverse Recovery Charge		-	110	-	nC
Dynamic Characteristics [b]						
C_{iss}	Input Capacitance	V_{DS}=40 V, V_{GS}=0 V, Frequency=1 MHz	-	6234	-	pF
C_{oss}	Output Capacitance		-	1180	-	
C_{rss}	Reverse Transfer Capacitance		-	97	-	
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=40 V, V_{GEN}=10 V, R_G=4.5 Ω, R_L=1.3 Ω, I_{DS}=30 A	-	41	-	ns
t_r	Turn-on Rise Time		-	68	-	
$t_{d(off)}$	Turn-off Delay Time		-	76	-	
t_f	Turn-off Fall Time		-	44	-	
Gate Charge Characteristics [b]						
Q_g	Total Gate Charge	V_{DS}=40 V, V_{GS}=10 V, I_{DS}=30 A	-	124	-	nC
Q_{gs}	Gate-Source Charge		-	31.2	-	
Q_{gd}	Gate-Drain Charge		-	39.2	-	

Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

7. Typical Characteristics

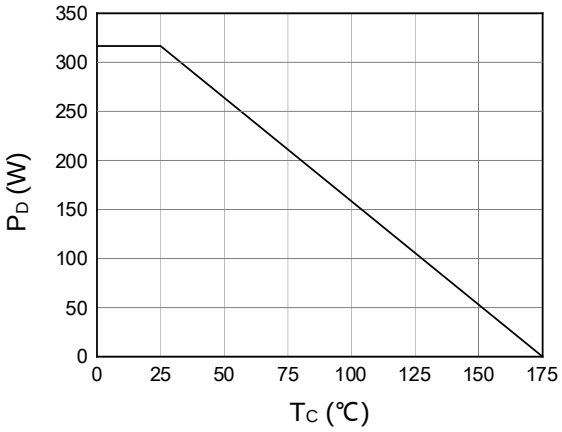


Figure 1. Power Capability

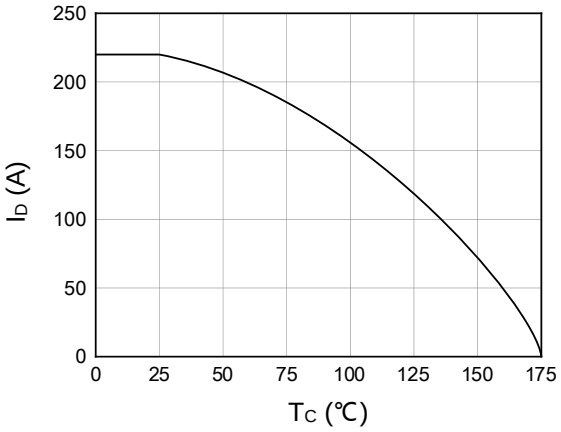


Figure 2. Current Capability

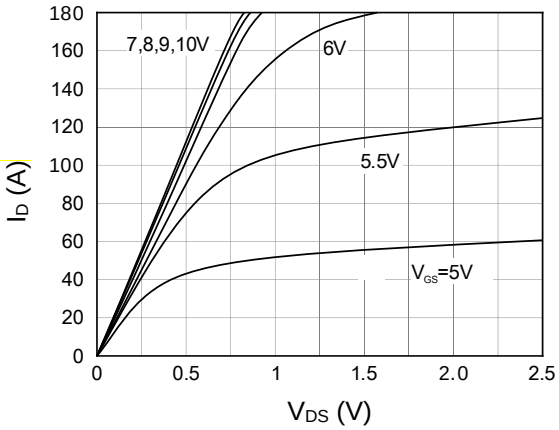


Figure 3. Output characteristics

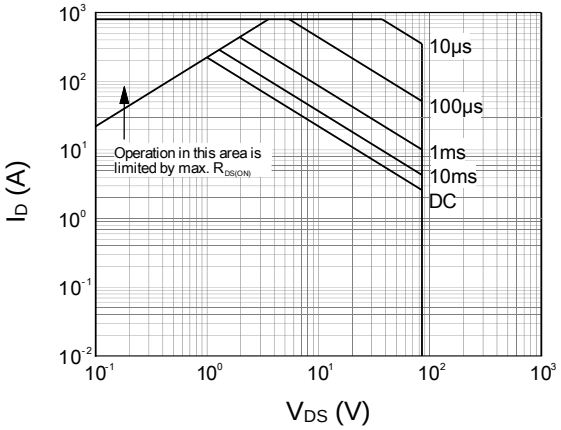


Figure 4. Safe operating area

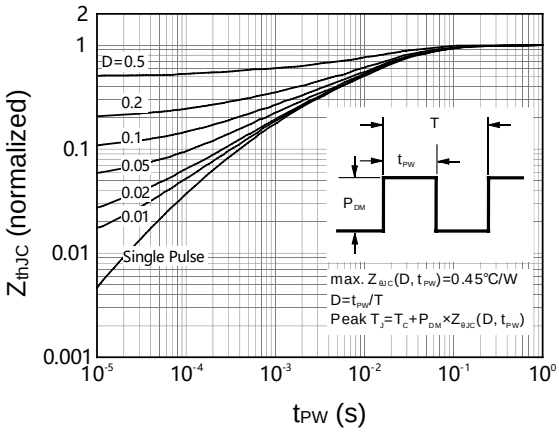


Figure 5. Normalized transient thermal impedance from junction to case

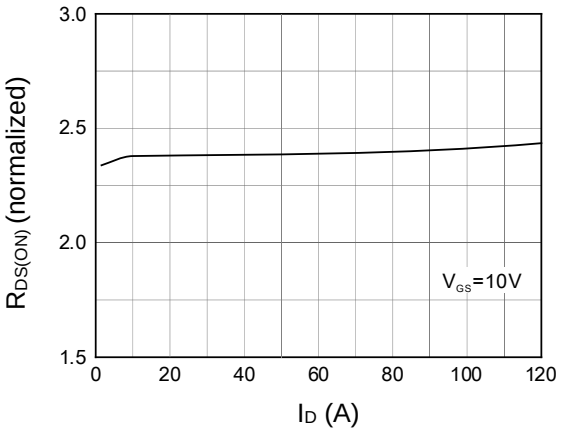


Figure 6. Normalized on-resistance vs drain current

7. Typical Characteristics (cont.)

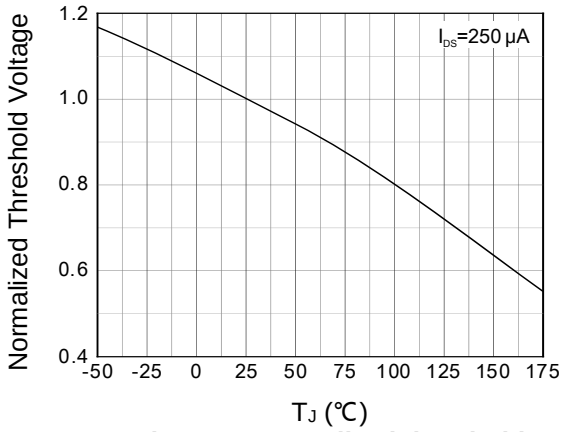


Figure 7. Normalized threshold voltage

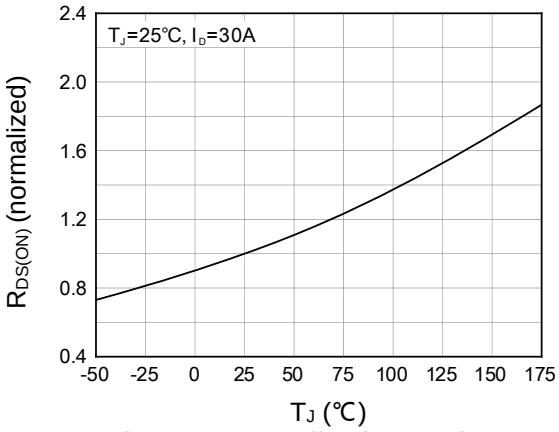


Figure 8. Normalized on-resistance vs junction temperature

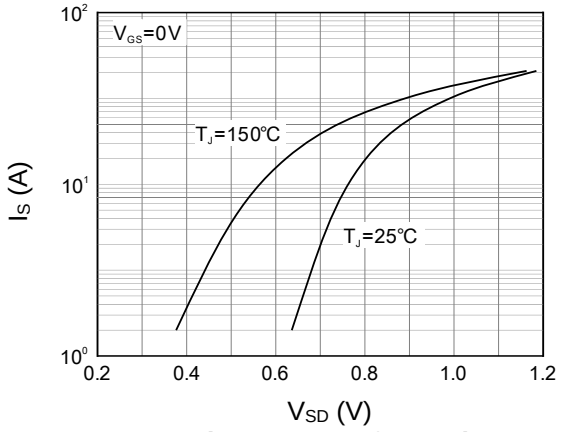


Figure 9. Typ. forward characteristics of body diode

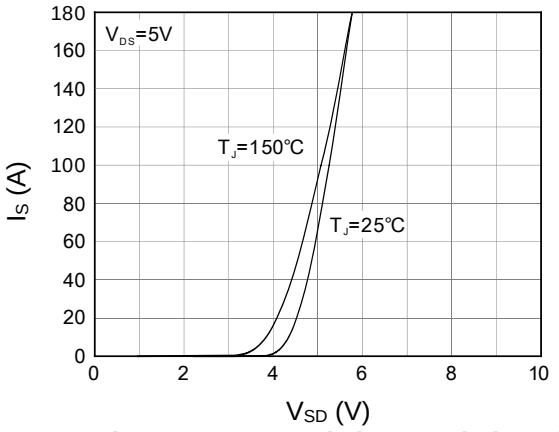


Figure 10. Forward characteristics of body diode

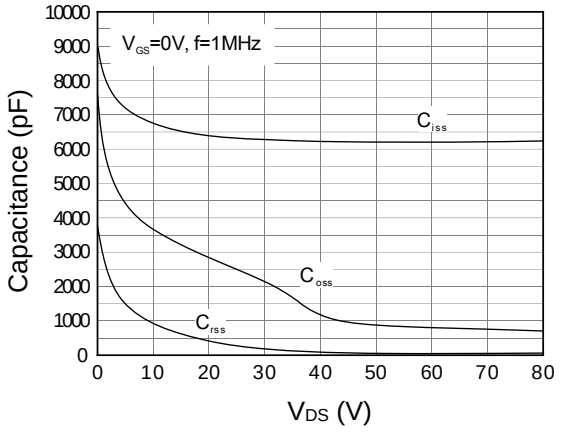


Figure 11. Capacitance

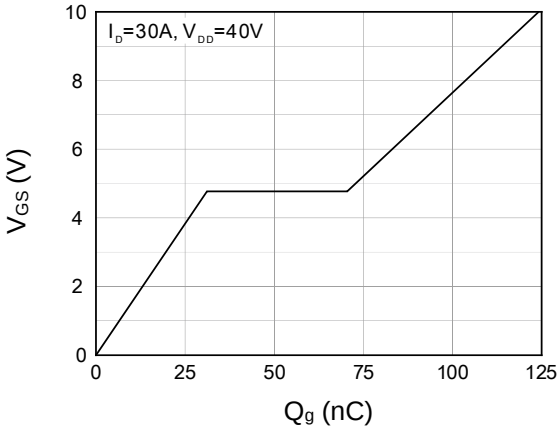


Figure 12. Gate charge

8. Test Circuit and Waveform

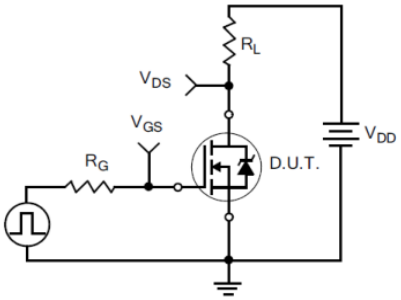


Figure 13. Resistive Switching Test Circuit

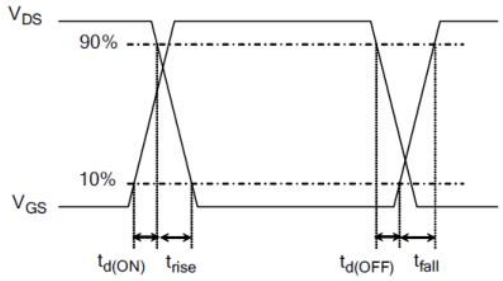


Figure 14. Resistive Switching Waveforms

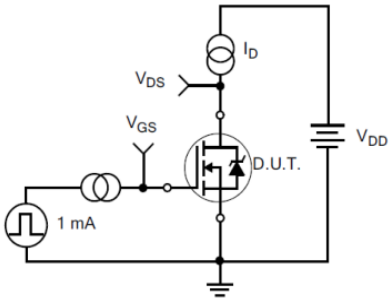


Figure 15. Gate Charge Test Circuit

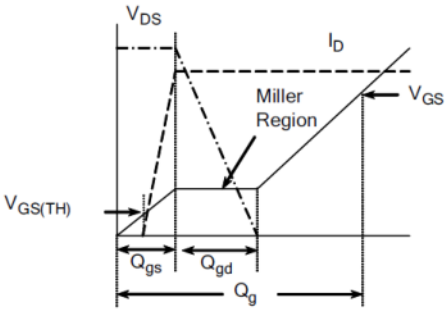


Figure 16. Gate Charge Waveforms

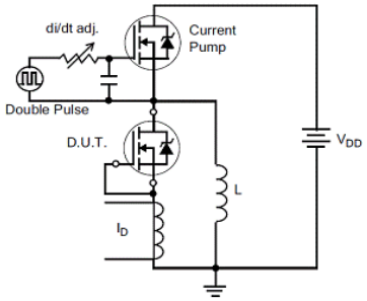


Figure 17. Diode Reverse Recovery Test Circuit

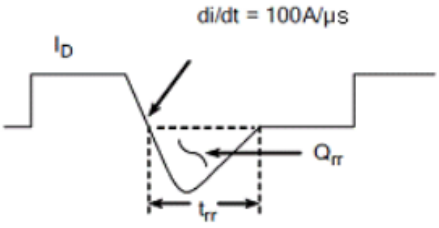


Figure 18. Diode Reverse Recovery Waveform

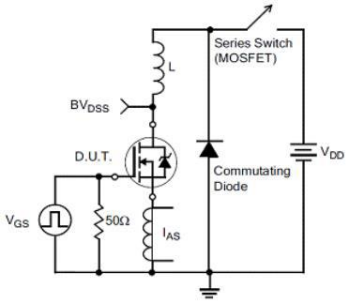


Figure 19. Diode Reverse Recovery Test Circuit

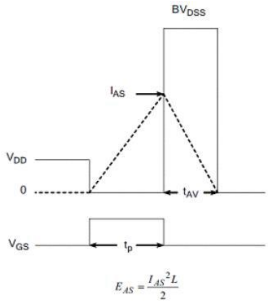
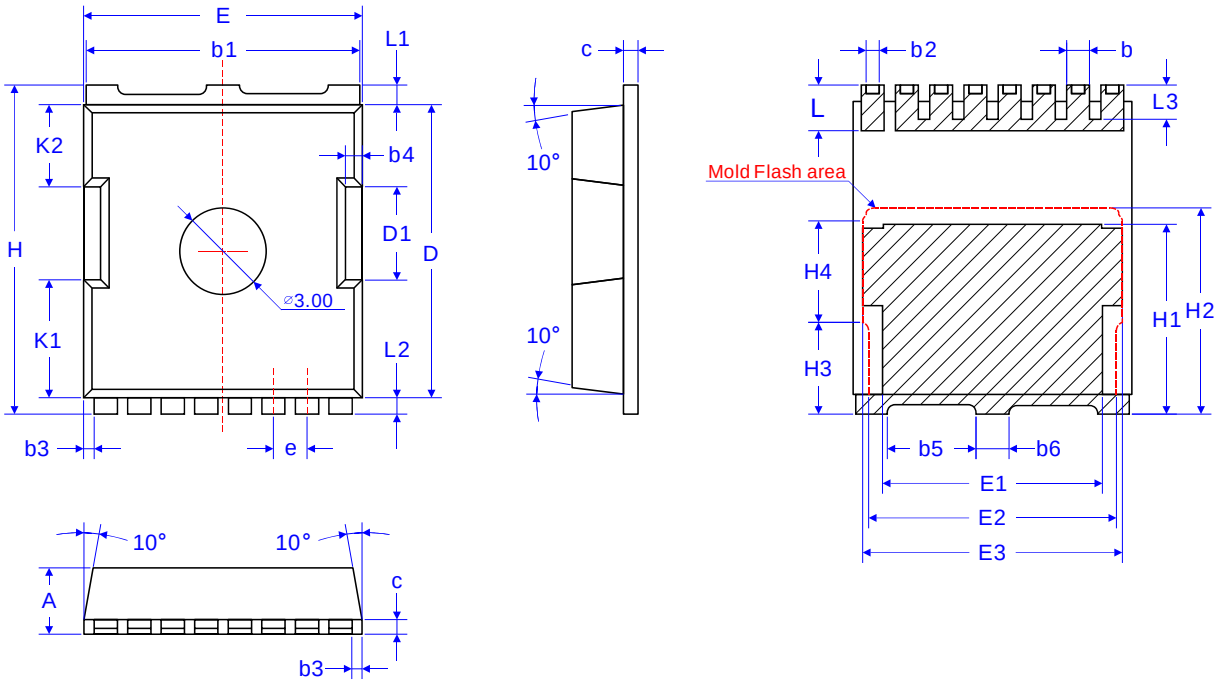


Figure 20. Diode Reverse Recovery Waveform

9. Package Dimensions

TOLL-8L Package



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.42	0.46	0.50
b3		0.35	
b4		0.60	
b5		3.10	
b6		1.20	
c	0.492	0.500	0.508
D	10.28	10.38	10.48
D1		3.30	
E	9.80	9.90	10.00
E1		7.80	
E2		8.80	

Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
E3		9.20	
e		1.20 BSC	
H	11.58	11.68	11.78
H1	6.65	6.75	6.85
H2		7.30	
H3		3.20	
H4		3.80	
K1		4.18	
K2		2.90	
L	1.70	1.90	2.10
L1		0.70	
L2		0.60	
L3	1.05	1.15	1.25