# KJ2060K

## N-Channel Enhancement Mode MOSFET

## 1. Product Information

### 1.1 Features

- ☑ Surface-mounted package
- ☑ Low gate charge

### 1.2 Applications

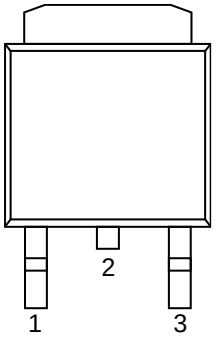
- ☑ Battery protection
- ☑ Uninterruptible power supply
- ☑ General purpose applications

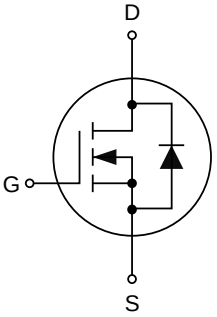
### 1.3 Quick reference

- ☑ BV ≥ 20 V
- ☑ $R_{DS(ON)}$ ≤ 6.0 mΩ @$V_{GS}$ = 4.5 V
- ☑ $P_{tot}$ ≤ 65 W
- ☑ $I_D$ ≤ 60 A

## 2. Pin Description

| Pin | Description |
|---|---|
| 1 | Gate |
| 2 | Drain |
| 3 | Source |




**Top View**
**TO-252**

## 3. Limiting Values

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | $T_C$=25℃ | - | 20 | V |
| $V_{GS}$ | Gate-Source Voltage | $T_C$=25℃ | - | ±12 | V |
| $I_D$* | Continuous drain current | $T_C$=25℃, $V_{GS}$=4.5 V | - | 60 | A |
| | | $T_C$=25℃, $V_{GS}$=4.5 V | - | 45 | |
| $I_{DM}$ *, **, *** | Pulsed Drain Current | $T_C$=25℃, $V_{GS}$=4.5 V | - | 210 | A |
| $E_{AS}$ | Avalanche energy, single pulse | $V_{DS}$=10 V, L=0.5 mH | - | 252 | mJ |
| $P_{tot}$ * | Total Power Dissipation | $T_C$=25℃ | - | 65 | W |
| $T_J$, $T_{stg}$ | Operating Junction and Storage Temperature Range | | -55 | 150 | ℃ |
| $R_{\theta JC}$ * | Thermal Resistance-Junction to Case | | - | 1.85 | ℃/W |

Notes:

* Pulse width ≤ 300 μs, duty cycle ≤ 2%.

** Mounted on PCB of 1 $in^2$ pad area.

*** Mounted on large heat sink.

## 4. Marking Information

| Product Name | Marking |
|---|---|
| KJ2060K | 2060K<br>YWWXXX<br>YWW: Date Code |

## 5. Ordering Code

| Product Name | Package | Reel size | Tape width | Quantity (pcs) |
|---|---|---|---|---|
| KJ2060K | TO-252 | 13" | 16 mm | 2500 |

Note: KUAIJIEXIN defines “Green” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C).

## 6. Electrical Characteristics ($T_C$=25℃ unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0 V, $I_{DS}$=250 μA | 20 | - | - | V |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_{DS}$=250 μA | 0.46 | 0.7 | 1.0 | V |
| $I_{DSS}$ | Zero Gate Voltage Source Current | $V_{DS}$=30 V, $V_{GS}$=0 V | - | - | 1 | μA |
| $I_{GSS}$ | Gate-source leakage current | $V_{GS}$=±20 V, $V_{DS}$=0 V | - | - | ±100 | nA |
| $R_{DS(ON)}$ [a] | Drain-Source On-State Resistance | $V_{GS}$=4.5 V, $I_{DS}$=20 A | - | 4.8 | 6.0 | mΩ |
| | | $V_{GS}$=2.5 V, $I_{DS}$=15 A | - | 6.7 | 11 | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$=5 V, $I_{DS}$=15 A | - | 35 | - | S |
| **Diode Characteristics** | | | | | | |
| $V_{SD}$ [a] | Diode Forward Voltage | $I_{SD}$=20 A, $V_{GS}$=0 V | - | - | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_{SD}$=20 A, $dI_{SD}/dt$=300 A/μs | - | 24 | - | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 12 | - | nC |
| **Dynamic Characteristics** [b] | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0 V, $V_{DS}$=15 V, Frequency=1 MHz | - | 2844 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 360 | - | |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 280 | - | |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DS}$=15 V, $V_{GS}$=4.5 V, $R_L$=0.75 Ω, $R_{GEN}$=3 Ω | - | 18 | - | ns |
| $t_r$ | Turn-on Rise Time | | - | 54 | - | |
| $t_{d(off)}$ | Turn-off Delay Time | | - | 77 | - | |
| $t_f$ | Turn-off Fall Time | | - | 25 | - | |
| **Gate Charge Characteristics** [b] | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{DS}$=15 V, $V_{GS}$=4.5 V, $I_{DS}$=12 A | - | 34 | - | nC |
| $Q_{gs}$ | Gate-Source Charge | | - | 4 | - | |
| $Q_{gd}$ | Gate-Drain Charge | | - | 14 | - | |

Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

# 7. Typical Characteristics

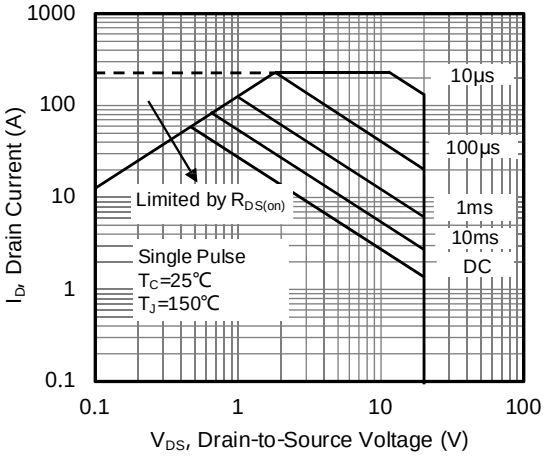



**Figure 1. Maximum Safe Operating Area**

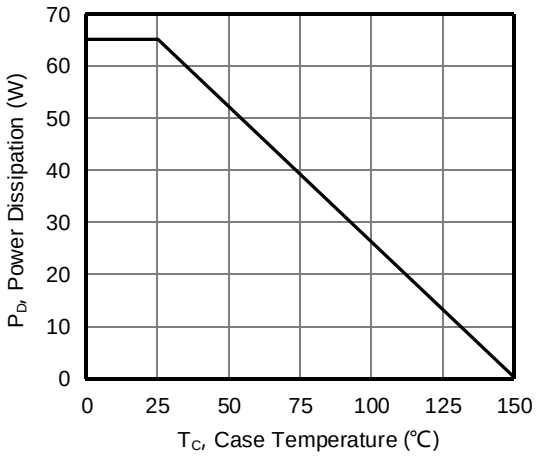



**Figure 2. Maximum Power Dissipation vs Case Temperature**

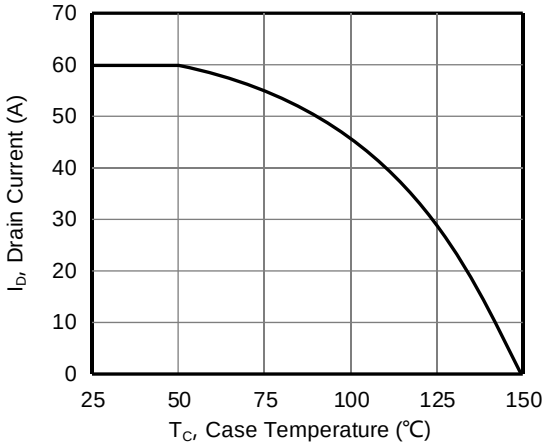



**Figure 3. Maximum Continuous Drain Current vs Case Temperature**

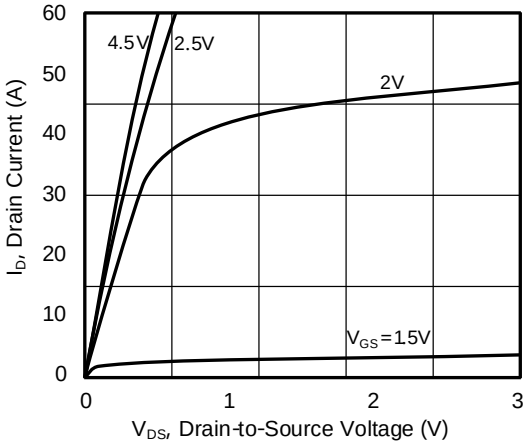



**Figure 4. Typical output Characteristics**

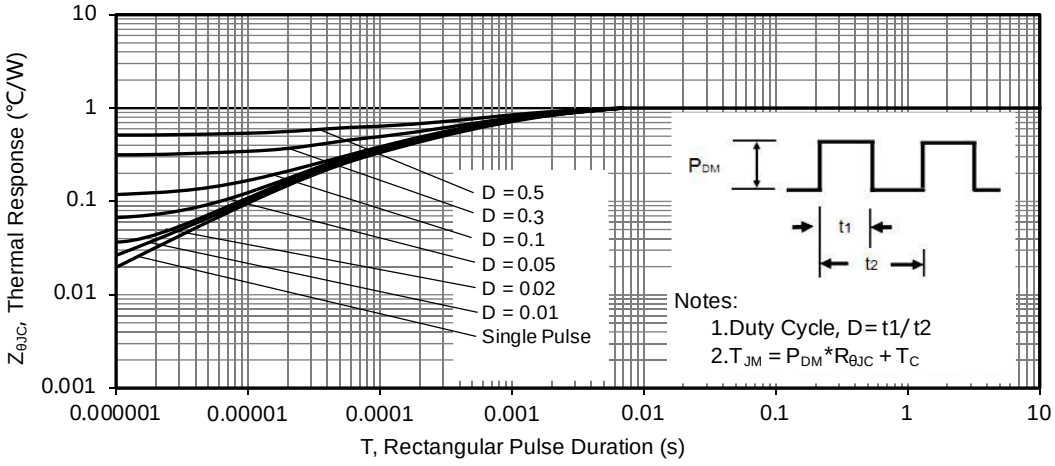



**Figure 5. Maximum Effective Thermal Impedance, Junction to Case**

# 7. Typical Characteristics (cont.)

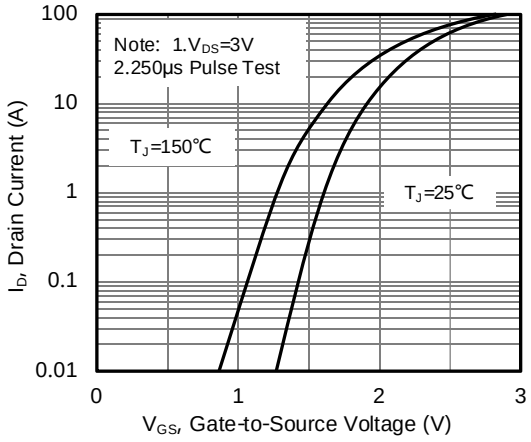



**Figure 6. Body-Diode Characteristics**

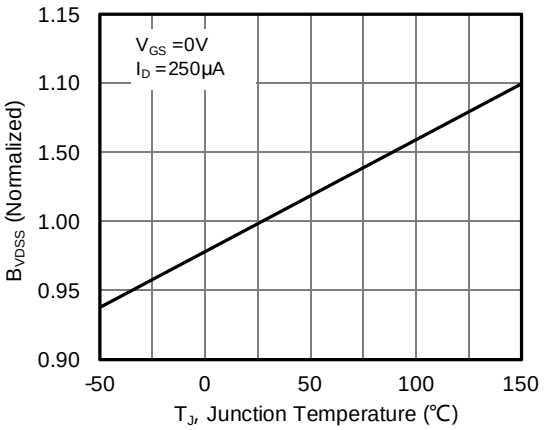



**Figure 7. Normalized Breakdown Voltage vs Junction Temperature**

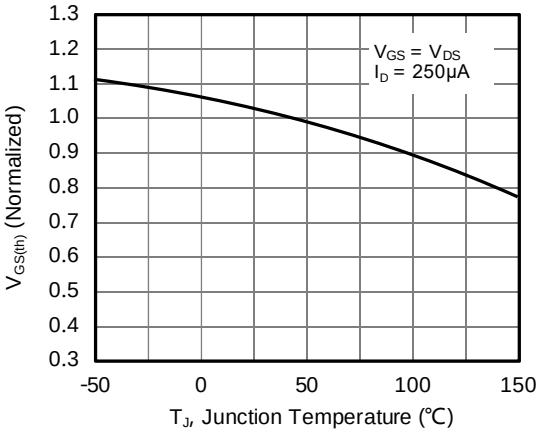



**Figure 8. Normalized Threshold Voltage vs Junction Temperature**

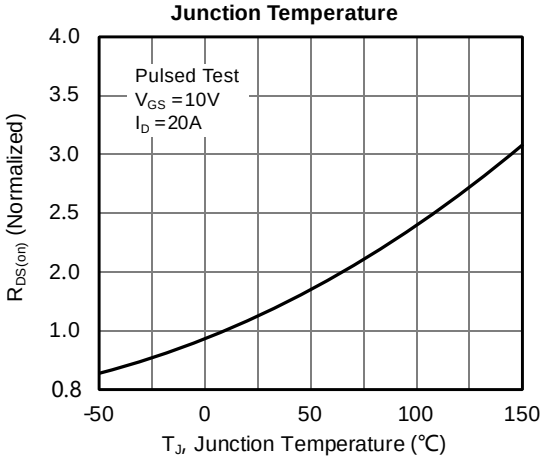



**Figure 9. Normalized On Resistance vs Junction Temperature**

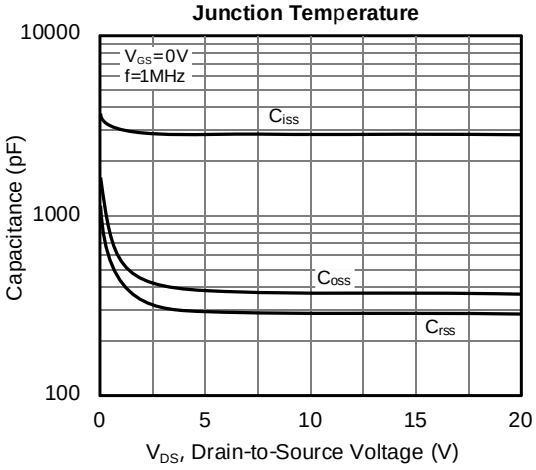



**Figure 10. Capacitance Characteristics**

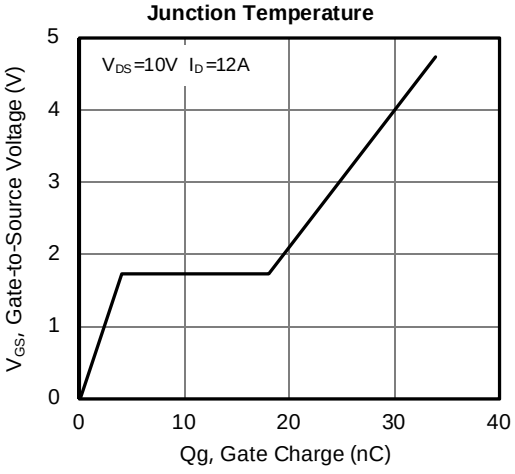
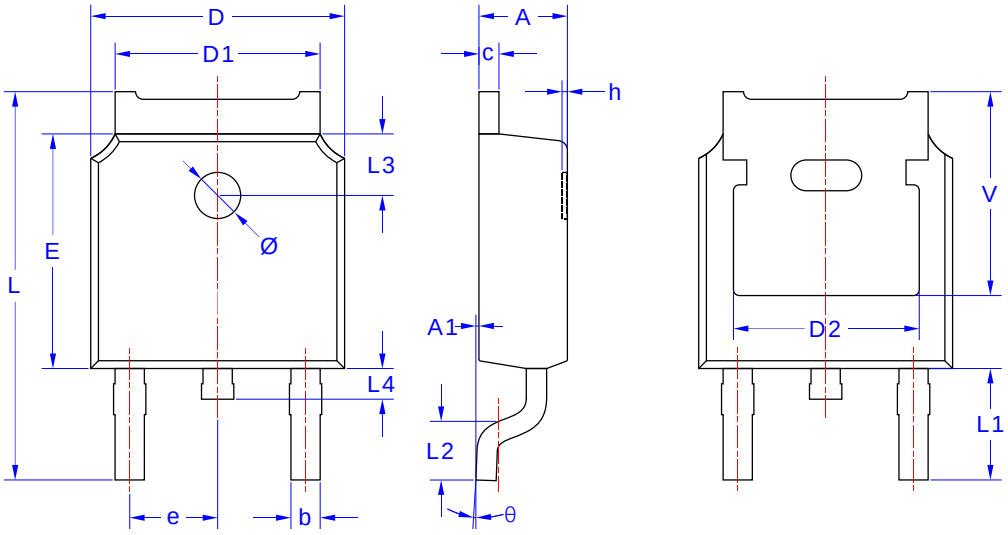



**Figure 11. Typical Gate Charge vs Gate to Source Voltage**

# 8. Package Dimensions

## TO-252 Package




| Symbol | Dimensions in Millimeters | |
|---|---|---|
| | MIN | MAX |
| A | 2.200 | 2.400 |
| A1 | 0 | 0.127 |
| b | 0.660 | 0.860 |
| c | 0.460 | 0.580 |
| D | 6.500 | 6.700 |
| D1 | 5.100 | 5.460 |
| D2 | 4.830 REF. | |
| E | 6.000 | 6.200 |
| e | 2.186 | 1.386 |
| L | 9.800 | 10.400 |
| L1 | 2.900 REF. | |
| L2 | 1.400 | 1.700 |
| L3 | 1.600 REF. | |
| L4 | 0.600 | 1.000 |
| ⌀ | 1.100 | 1.300 |
| θ | 0° | 8° |
| H | 0 | 0.300 |
| V | 5.350 REF. | |