KJ9435A

P-Channel Enhancement Mode MOSFET

1. Product Information

Features

- Advanced trench cell design
- Excellent $R_{DS(ON)}$ and Low Gate

Applications

- Battery protection
- Load switch
- Uninterruptible power supply

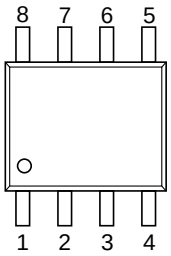
Quick reference

- $B_V \geq -30$ V
- $P_{tot} \leq 2.15$ W
- $I_D \leq -6$ A
- $R_{DS(ON)} \leq 55\ m\Omega$ @$V_{GS} = 10$ V

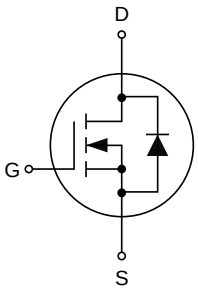
Pin Description

Pin	Description
1,2,3	Source(S)
4	Gate(G)
5,6,7,8	Drain(D)

Simplified Outline	Symbol



Top View
SOP8



Package Marking and Ordering Information

Product Name	Package	Marking	Reel size	Tape width	Quantity (pcs)
KJ9435A	SOP-8L	9435A XXXXXX	13"	12 mm	3000

2. Absolute Maximum Ratings (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @-10V [1]	-6.0	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @-10V [1]	-3.3	A
I_{DM}	Pulsed Drain Current [1]	-20.4	A
P_D	Power Dissipation T_A = 25℃	2.15	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	58	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃

3. Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= -250μA	-30	-33	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -30V, V_{GS} = 0V,	-	-	-1	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS} =0V, V_{GS} = ±20V	-	-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D= -250μA	-1.0	-1.6	-2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance note2	V_{GS} =-10V, I_D =-5A	-	43	55	mΩ
		V_{GS} =-4.5V, I_D =-4A	-	65	90	
C_{iss}	Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1.0MHz	-	596	-	pF
C_{oss}	Output Capacitance		-	95	-	pF
C_{rss}	Reverse Transfer Capacitance		-	68	-	pF
Q_g	Total Gate Charge	V_{DS}= -15V, I_D = -5.1A, V_{GS} = -10V	-	6.8	-	nC
Q_{gs}	Gate-Source Charge		-	1	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	1.4	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = -15V, I_D = -1A, V_{GS}=-10V, R_{GEN}=2.5Ω	-	14	-	ns
t_r	Turn-on Rise Time		-	61	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	19	-	ns
t_f	Turn-off Fall Time		-	10	-	ns
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-5.1	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-20.4	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_S = -5.1A	-	-0.8	-1.2	V

Note:

1. Surface mounted on a 1 inch^2 FR-4 board with 2 OZ copper.
2. Pulse width ≦ 300 us , duty cycle ≦ 2%.
3. EAS test condition is V_{DD}=-25 V, V_{GS}=-10 V, L=0.1 mH, I_{AS}=-5 A.
4. P_D is limited by 150℃ junction temperature.
5. The data is theoretically the same as I_D and I_{DM}, in real applications , should be limited by total power dissipation.

4.Typical Characteristics

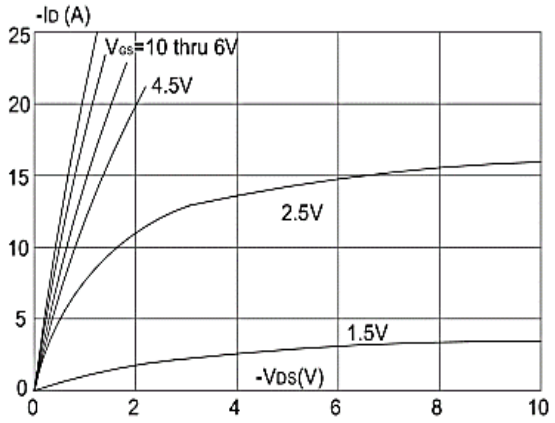


Figure1: Output Characteristics

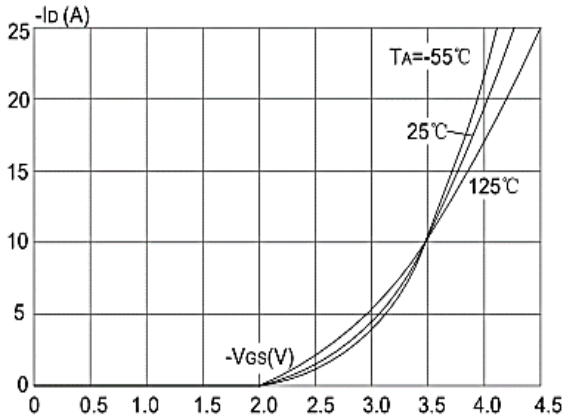


Figure 2: Typical Transfer Characteristics

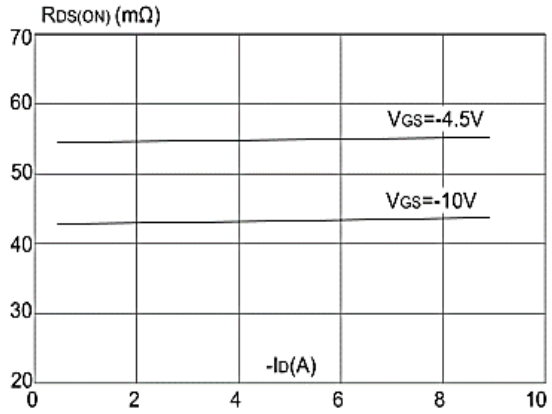


Figure 3:On-resistance vs. Drain Current

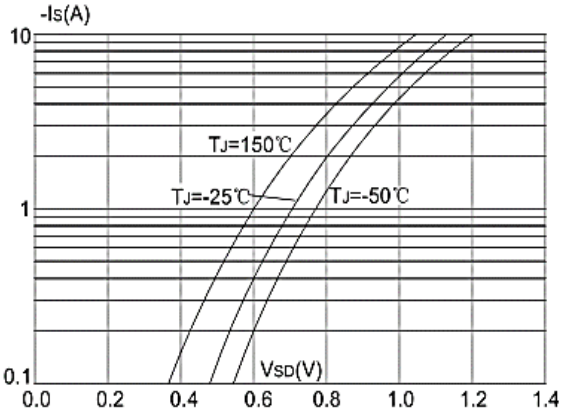


Figure 4: Body Diode Characteristics

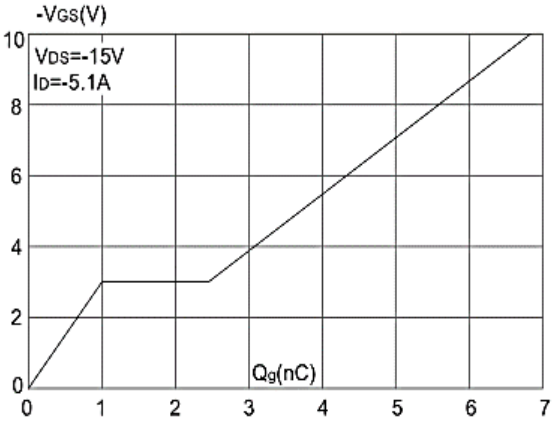


Figure 5: Gate Charge Characteristics

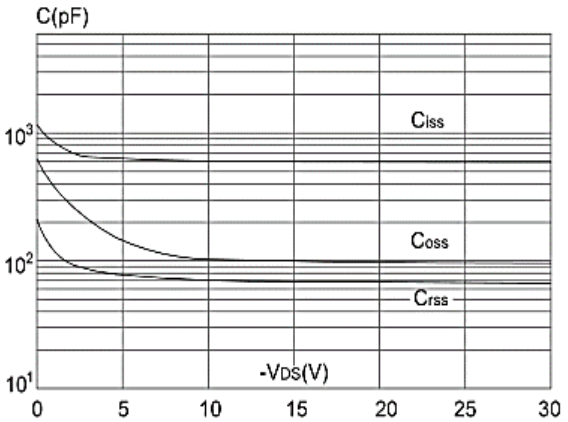


Figure 6: Capacitance Characteristics

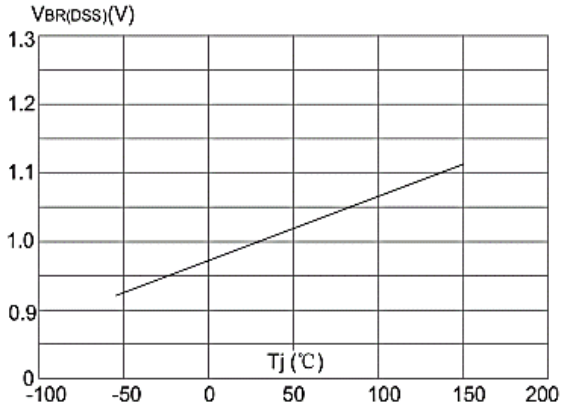


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

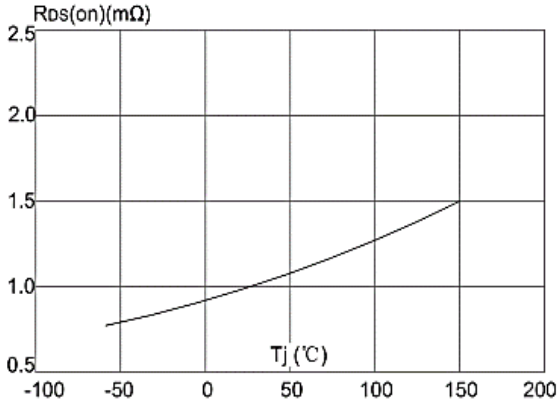


Figure 8: Normalized on Resistance vs Junction Temperature

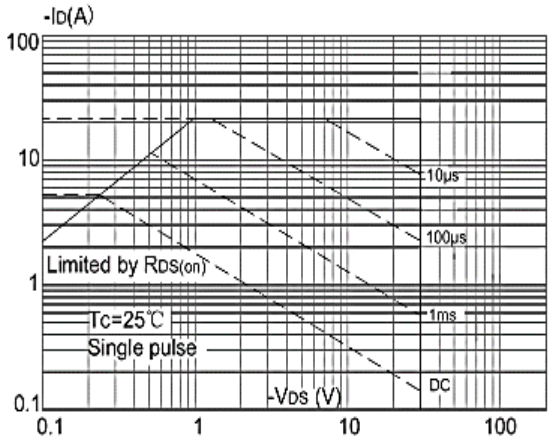


Figure 9: Maximum Safe Operating Area vs. Case Temperature

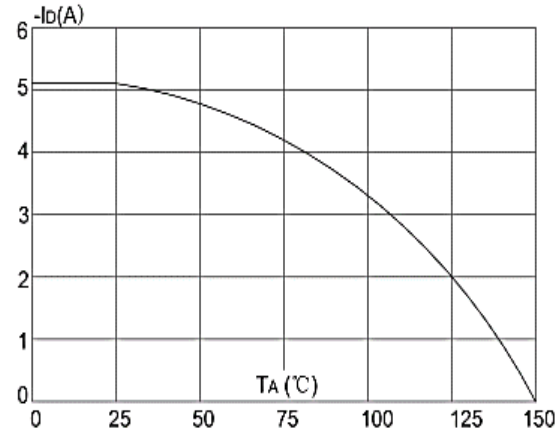


Figure 10: Maximum Continuous Drain Current

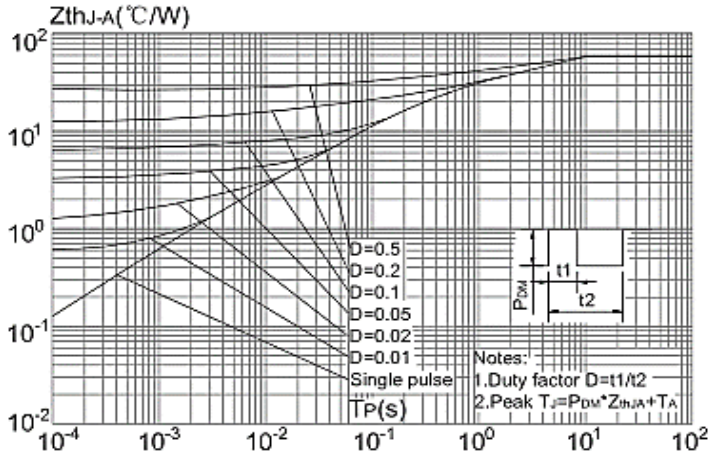
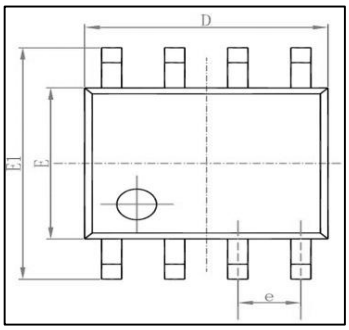
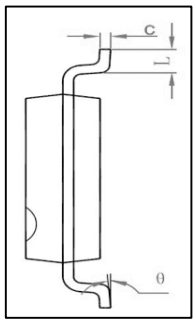


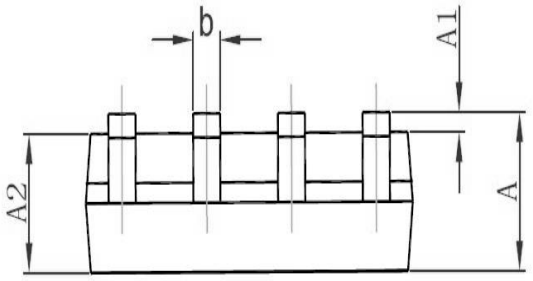
Figure.11: Maximum Effective

5. Package Mechanical Data

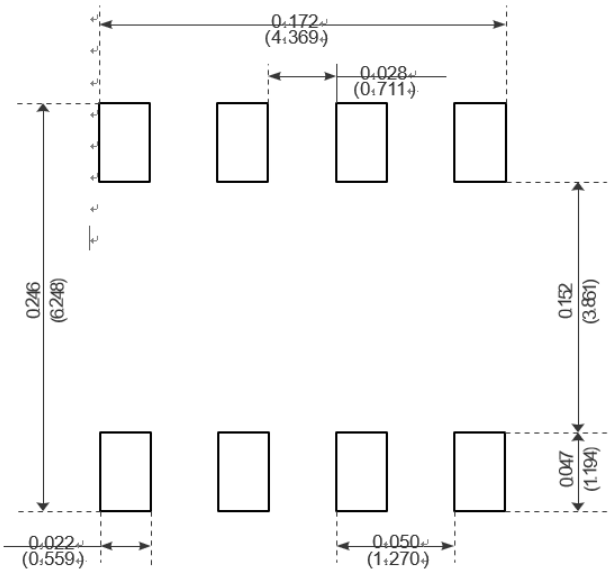
SOP-8L Package







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads