

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ✓ Advanced trench cell design
- ✓ Super Trench
- ✓ T_J max 175°C
- ✓ Low Thermal Resistance
- ✓ MSL1

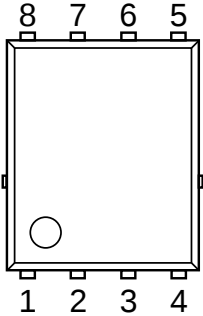
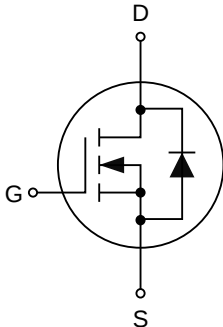
1.2 Applications

- ✓ Motor drivers
- ✓ DC/DC Converter

1.3 Quick reference

- ✓ $BV \geq 40$ V
- ✓ $P_{tot} \leq 188$ W
- ✓ $I_D \leq 289$ A
- ✓ $R_{DS(ON)} \leq 1.0$ m Ω @ $V_{GS} = 10$ V

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1,2,3	Source	 Top View PDFN5x6-8L	
4	Gate		
5,6,7,8	Drain		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_C=25^{\circ}\text{C}$	40	-	V
V_{GS}	Gate-Source Voltage	$T_C=25^{\circ}\text{C}$	-	± 20	V
$I_D^{*,***}$	Drain Current	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	289	A
$I_D^{*,***}$	Drain Current	$T_C=100^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	204	A
$I_{DM}^{*,**,***}$	Pulsed Source Current	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	867	A
P_{tot}^{*}	Total Power Dissipation	$T_C=25^{\circ}\text{C}$	-	188	W
T_J, T_{stg}	Operating Junction and Storage Temperature		-55	175	$^{\circ}\text{C}$
I_S	Diode Forward Current	$T_C=25^{\circ}\text{C}$	-	289	A
E_{AS}	Single Pulsed Avalanche Energy	$V_{DD}=32\text{ V}, L=0.3\text{ mH}$	-	844	mJ
$R_{\theta JA}^{*}$	Thermal Resistance-Junction to Ambient		-	44	$^{\circ}\text{C/W}$
$R_{\theta JC}^{*}$	Thermal Resistance-Junction to Case		-	0.8	

Notes:

- * Surface mounted on 1 in² pad area, $t \leq 10\text{ sec.}$
- ** Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- *** Limited by bonding wire.

4. Marking Information

Product Name	Marking
KJ007N04G	KJ007N04G XXXXXX

5. Ordering Code

Product Name	Package	Reel size	Tape width	Quantity (pcs)
KJ007N04G	PDFN 5×6-8L	13"	12 mm	5000

Note: KUAJIEXIN defines "Green" as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C).

6. Electrical Characteristics (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0 V, I _{DS} =250 μA	40	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250 μA	1.2	1.7	2.2	V
I _{DSS}	Zero Gate Voltage Source Current	V _{DS} =40 V, V _{GS} =0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{GS} =±20 V, V _{DS} =0 V	-	-	±100	nA
R _{DS(ON)} ^a	Drain-Source On-State Resistance	V _{GS} =10 V, I _{DS} =50 A	-	0.7	1.0	mΩ
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} =1A, V _{GS} =0 V	-	0.75	1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} =50 A, dI _{SD} /dt=100 A/μs	-	65	-	ns
Q _{rr}	Reverse Recovery Charge		-	135	-	nC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{GS} =0 V, V _{DS} =20 V, Frequency=1 MHz	-	9450	-	pF
C _{oss}	Output Capacitance		-	2430	-	
C _{rss}	Reverse Transfer Capacitance		-	285	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} =20 V, V _{GEN} =10 V, R _G =3 Ω, I _{DS} =50 A	-	28	-	ns
t _r	Turn-on Rise Time		-	36	-	
t _{d(off)}	Turn-off Delay Time		-	99	-	
t _f	Turn-off Fall Time		-	46	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} =20 V, V _{GS} =10 V, I _{DS} =50 A	-	158	-	nC
Q _{gs}	Gate-Source Charge		-	33	-	
Q _{gd}	Gate-Drain Charge		-	42	-	

Notes:

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

7. Typical Characteristics

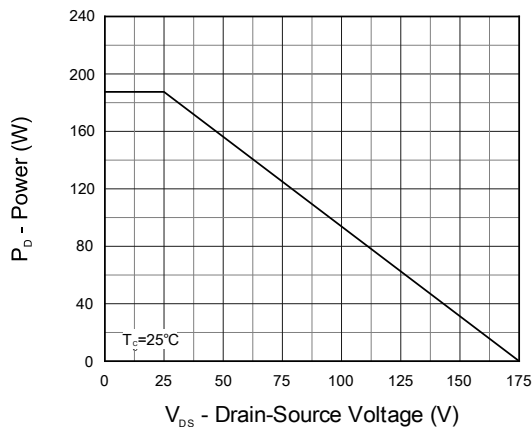


Figure 1. Power Capability

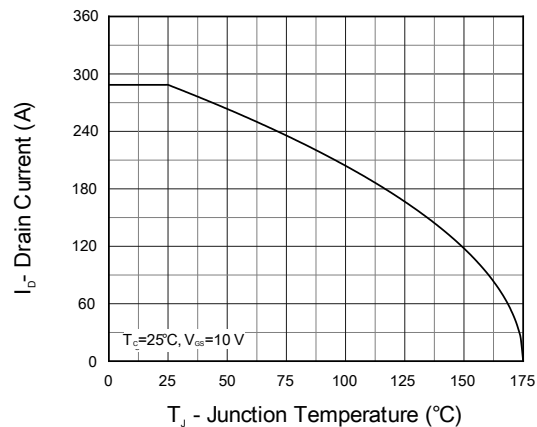


Figure 2. Current Capability

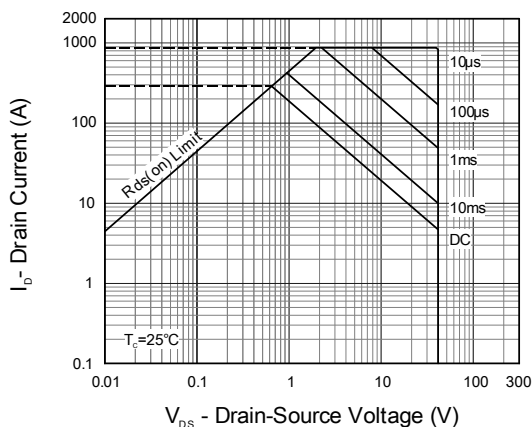


Figure 3. Safe Operation Area

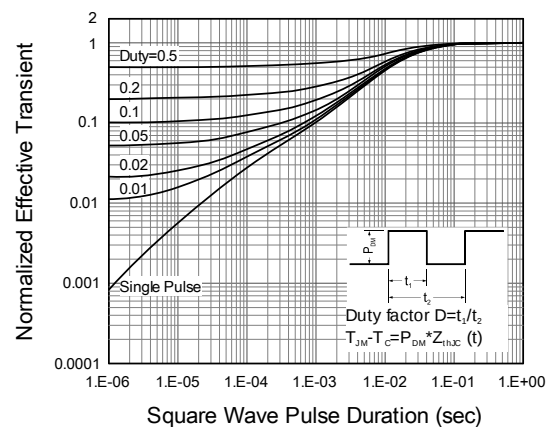


Figure 4. Transient Thermal Impedance

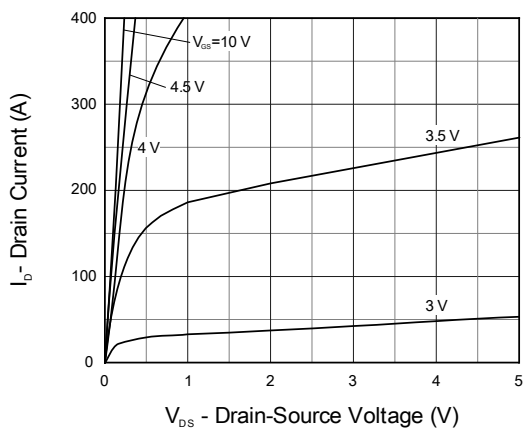


Figure 5. Output Characteristics

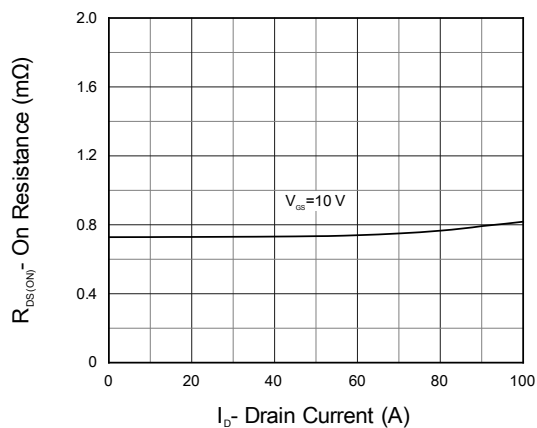


Figure 6. On Resistance

7. Typical Characteristics (cont.)

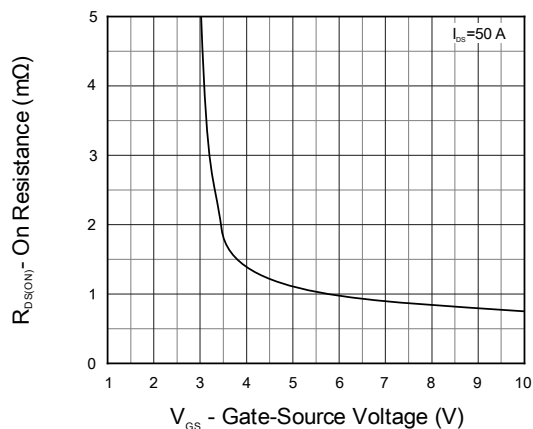


Figure 7. Transfer Characteristics

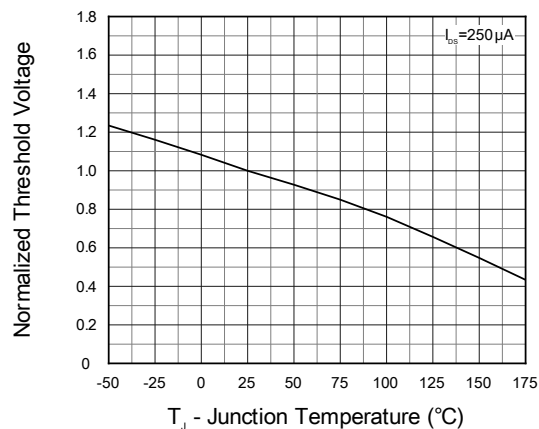


Figure 8. Normalized Threshold Voltage

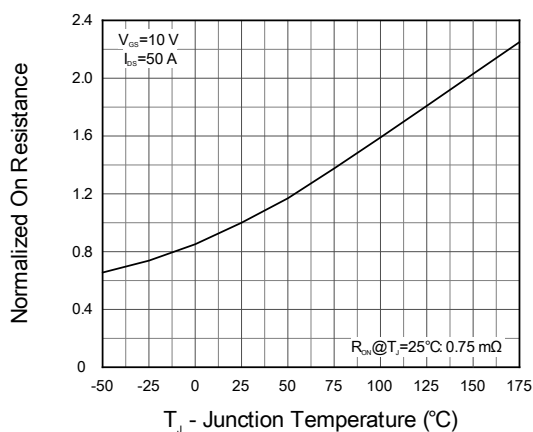


Figure 9. Normalized On Resistance

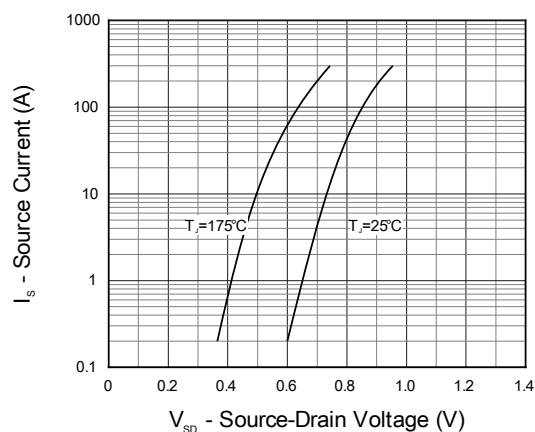


Figure 10. Diode Forward Current

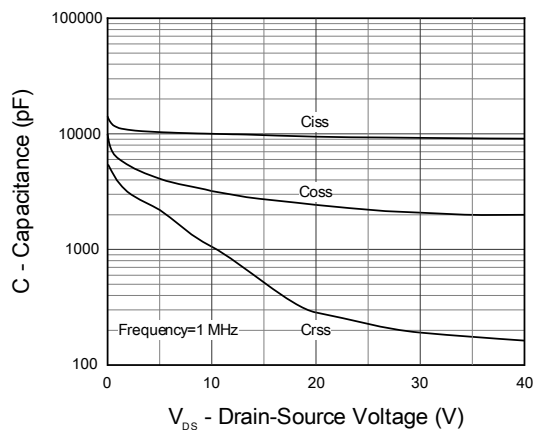


Figure 11. Capacitance

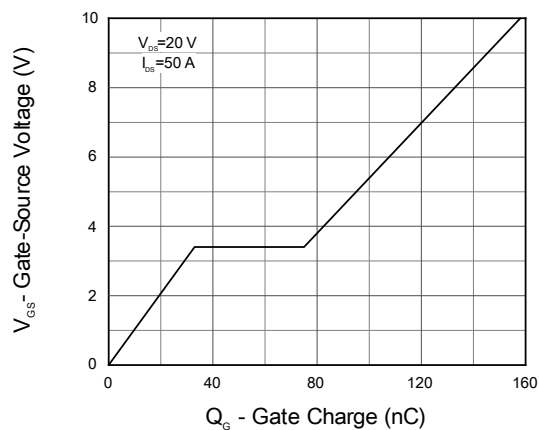
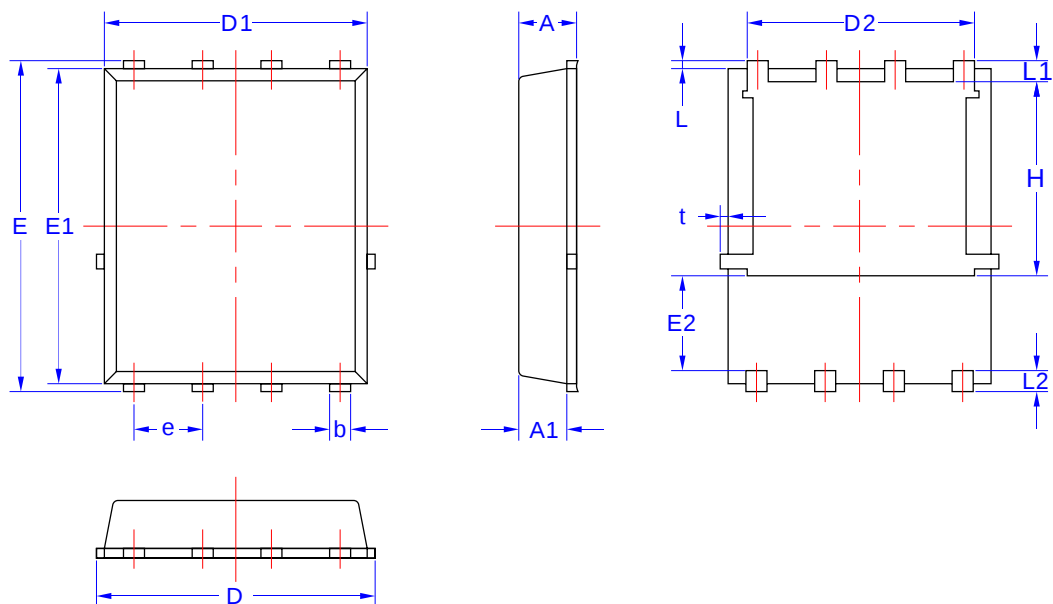


Figure 12. Gate Charge

8. Package Dimensions

PDFN 5×6-8L Package



Symbol	Dimensions in Millimeters	
	MIN.	MAX
A	1.03	1.17
A1	0.824	0.97
b	0.34	0.48
D	4.80	5.40
D1	4.80	5.00
D2	4.11	4.31
E	5.95	6.15
E1	5.65	5.85
E2	1.40	-
e	1.27 BSC	
L	0.05	0.25
L1	0.38	0.50
L2	0.38	0.71
H	3.30	3.50
t	-	0.18