

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☒ Advanced trench cell design
- ☒ Low thermal impedance
- ☒ Fast switching speed
- ☒ 100% avalanche tested

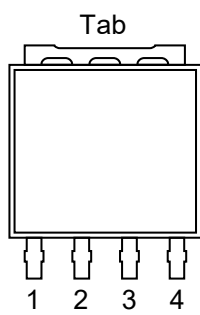
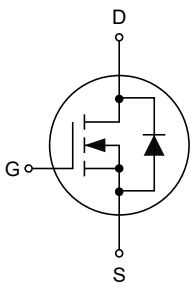
1.2 Applications

- ☒ DC/DC converter
- ☒ Power switch
- ☒ Motor drives

1.3 Quick reference

- ☒ $BV \geq 60\text{ V}$
- ☒ $P_{tot} \leq 156\text{ W}$
- ☒ $I_D \leq 307\text{ A}$
- ☒ $R_{DS(ON)} \leq 1.0\text{ m}\Omega @ V_{GS} = 10\text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1,2,3	Source	 Top View LFPAK 5×6	
4	Gate		
Tab	Drain		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_C=25^{\circ}\text{C}$	60	-	V
V_{GS}	Gate-Source Voltage	$T_C=25^{\circ}\text{C}$	-	± 20	V
I_D	Continuous Drain Current	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}^{[1]}$	-	307	A
		$T_C=100^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	194	A
I_{DM}	Pulsed Drain Current ^[2]	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	1228	A
P_D	Power Dissipation	$T_C=25^{\circ}\text{C}$	-	156	W
		$T_A=25^{\circ}\text{C}^{[3]}$	-	3.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55	150	$^{\circ}\text{C}$
E_{AS}	Single Pulsed Avalanche Energy	$V_{DD}=30\text{ V}, L=0.3\text{ mH}$	-	960	mJ
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		-	40	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case		-	0.8	

Notes:

1. Package limited.

2. Pulse width limited by maximum junction temperature.

3. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5"x1.5" board of FR-4 material.

4. Marking Information

Product Name	Marking
KJ011N06LFH	KJ011N06LFH XXXXXX-X

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity(pcs)
KJ011N06LFH	LFPK 5×6	13"	12 mm	5000

Note: KUAJIEXIN defines "Green" as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C)

6. Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0 V, I _{DS} =250 μA	60	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250 μA	2	-	4	V
I _{DSS}	Drain Leakage Current	V _{DS} =60 V, V _{GS} =0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{GS} =0 V, V _{GS} =±20 V	-	-	±100	nA
R _{DS(ON)}	On-State Resistance ^a	V _{GS} =10 V, I _{DS} =20 A	-	0.85	1.0	mΩ
g _{FS}	Forward Transconductance ^b	V _{GS} =5 V, I _{DS} =20 A	-	75	-	S
R _g	Gate Resistance	Frequency=1 MHz	-	2	-	Ω
Diode Characteristics						
V _{SD}	Diode Forward Voltage ^a	I _{SD} =20 A, V _{GS} =0 V	-	0.7	1.2	V
t _{rr}	Reverse Recovery Time	V _{DS} =30 V, I _{DS} =20 A, dI _{SD} /dt=100 A/μs	-	90	-	ns
Q _{rr}	Reverse Recovery Charge		-	190	-	nC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{GS} =0 V, V _{DS} =30 V, Frequency=1 MHz	-	7450	-	pF
C _{oss}	Output Capacitance		-	3400	-	
C _{rss}	Reverse Transfer Capacitance		-	175	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} =30 V, V _{GEN} =10 V, R _G =3 Ω, I _{DS} =20 A	-	12	-	ns
t _r	Turn-on Rise Time		-	30	-	
t _{d(off)}	Turn-off Delay Time		-	90	-	
t _f	Turn-off Fall Time		-	40	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} =30 V, V _{GS} =10 V, I _{DS} =20 A	-	96	-	nC
Q _{gs}	Gate-Source Charge		-	32	-	
Q _{gd}	Gate-Drain Charge		-	30	-	

Notes:

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

7. Typical Characteristics

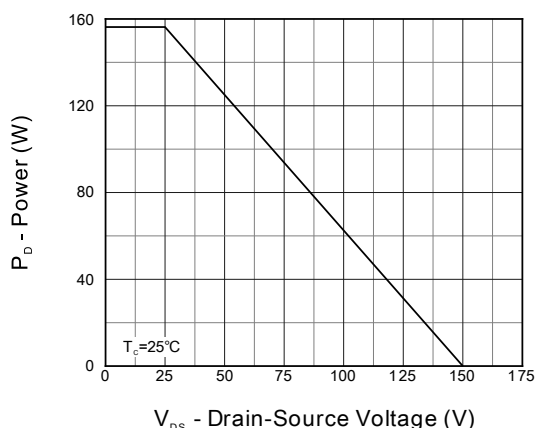


Figure 1. Output Characteristics

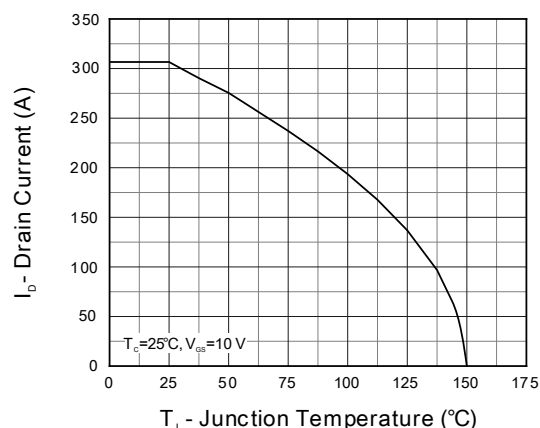


Figure 2. Current Capability

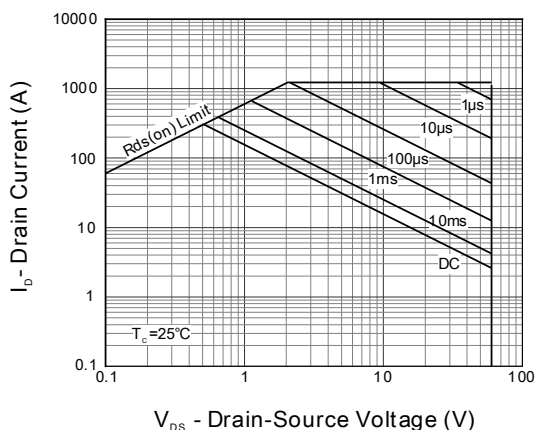


Figure 3. Safe Operation Area

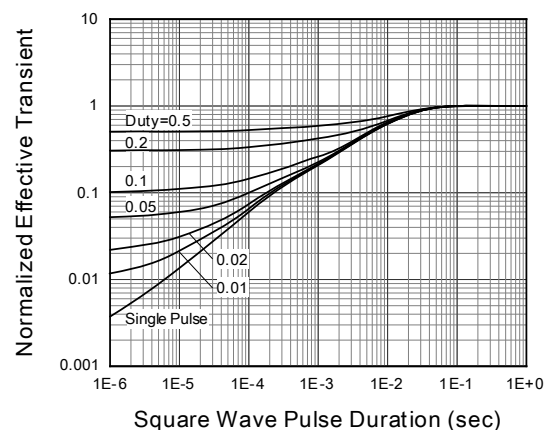


Figure 4. Transient Thermal Impedance

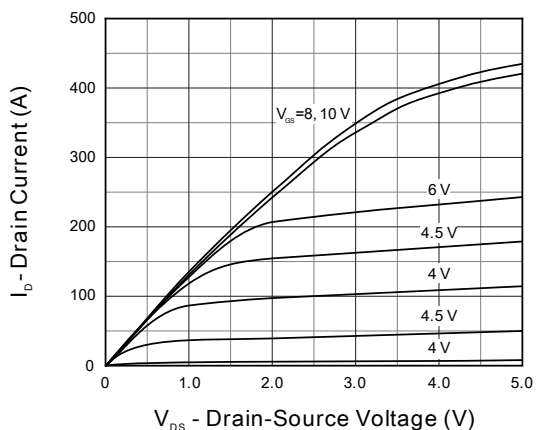


Figure 5. Output Characteristics

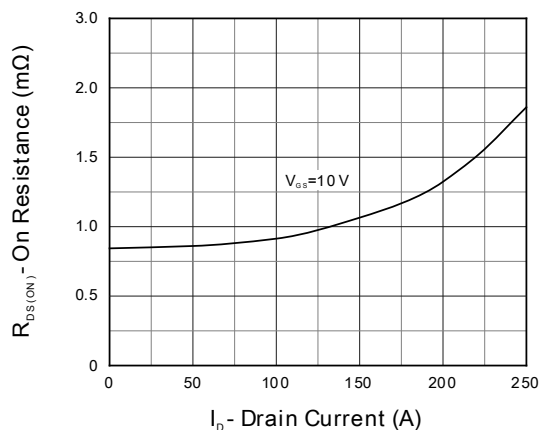


Figure 6. On Resistance

7. Typical Characteristics (cont.)

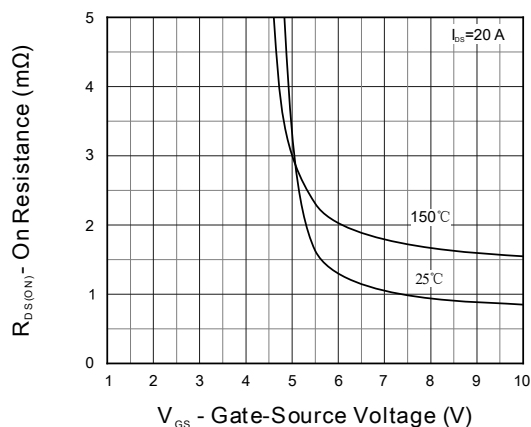


Figure 7. Transfer Characteristics

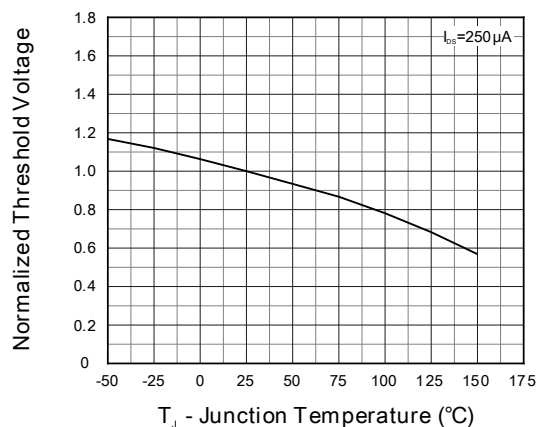


Figure 8. Normalized Threshold Voltage

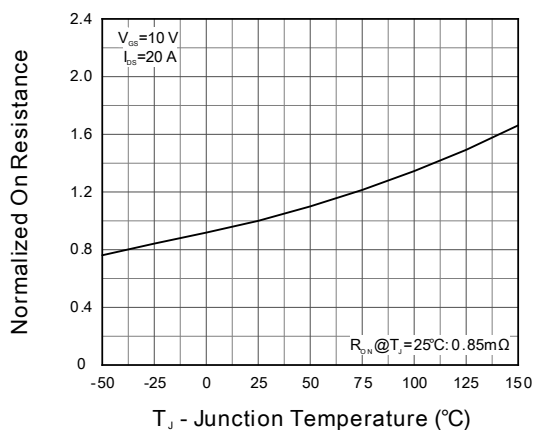


Figure 9. Normalized On Resistance

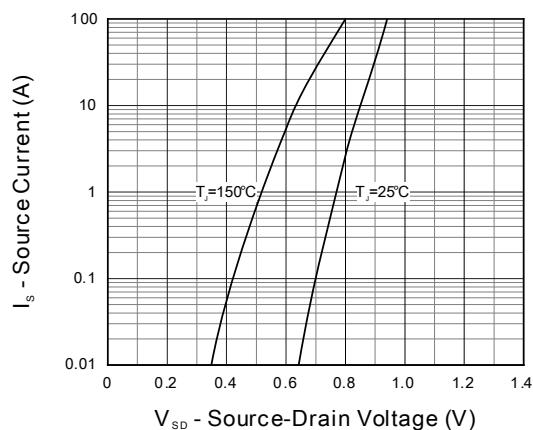


Figure 10. Diode Forward Current

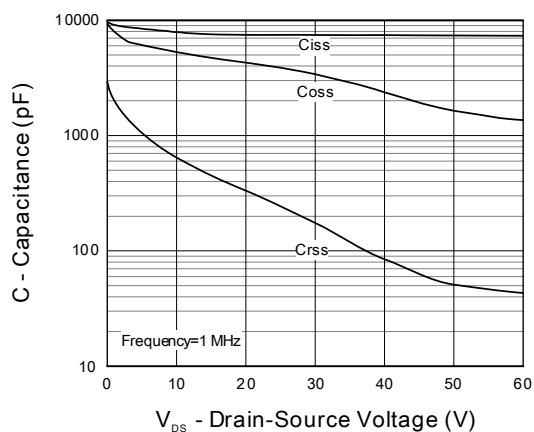


Figure 11. Capacitance

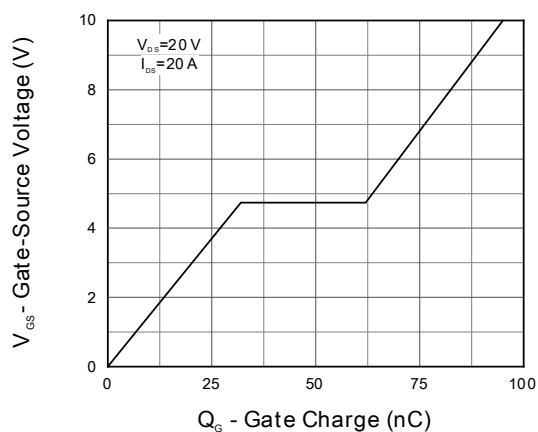
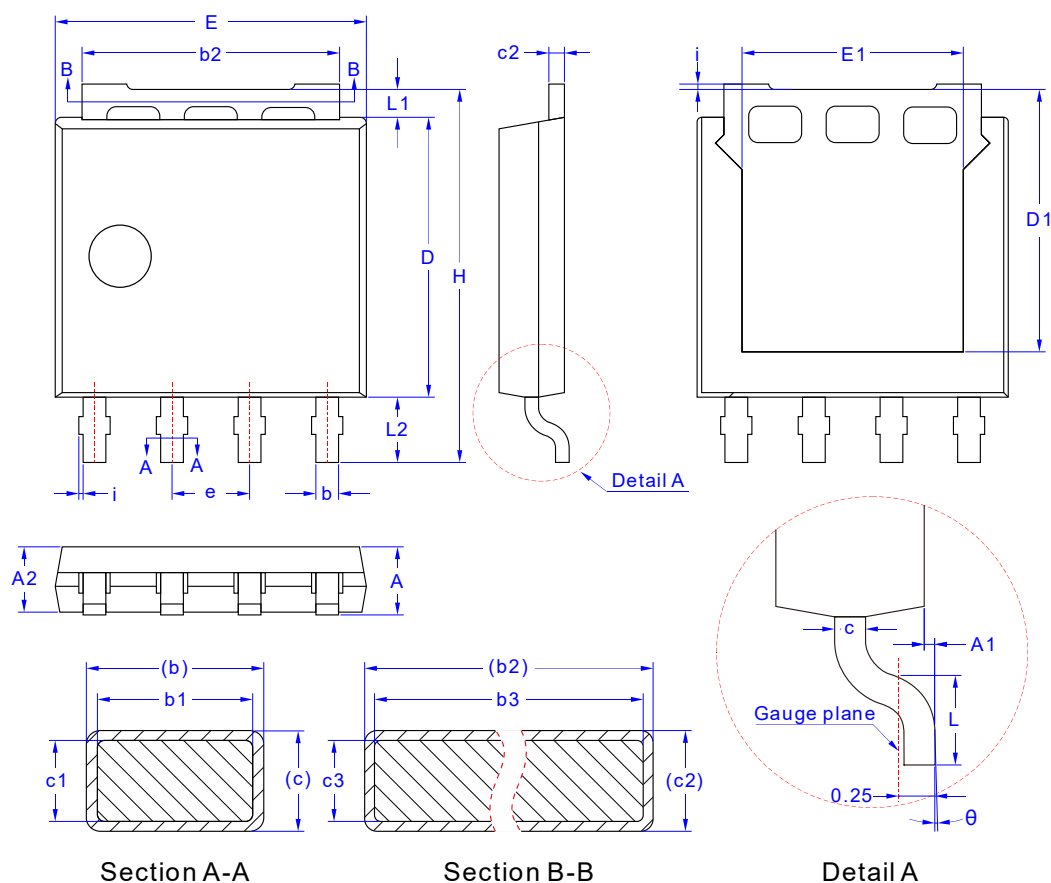


Figure 12. Gate Charge

8. Package Dimensions

LFPACK 5×6 Package



Symbol	Dimensions in Millimeters	
	MIN	MAX
A	1.00	1.30
A1	0	0.15
A2	0.98	1.12
b	0.35	0.50
b1	0.32	0.46
b2	4.02	4.41
b3	4.00	4.37
c	0.19	0.25
c1	0.17	0.23
c2	0.24	0.30
c3	0.22	0.28

Symbol	Dimensions in Millimeters	
	MIN	MAX
D	4.45	4.70
D1	-	4.45
E	4.95	5.30
E1	3.50	3.70
e	1.27 BSC	
H	5.95	6.25
i	-	0.25
L	0.40	0.85
L1	0.27	0.57
L2	0.80	1.30
θ	0°	8°