

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Surface-mounted package
- ☑ 100% Avalanche Tested
- ☑ $T_J \text{ max } 175^\circ\text{C}$
- ☑ Advanced trench cell design
- ☑ MSL1

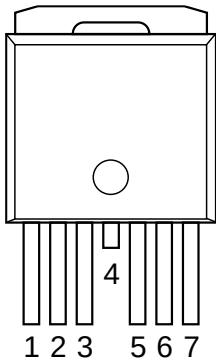
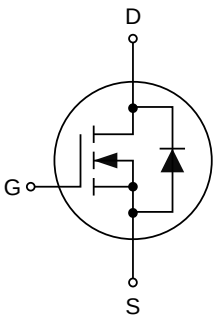
1.2 Applications

- ☑ Power Tool appliances
- ☑ BMS appliances
- ☑ High power inverter system

1.3 Quick reference

- ☑ $BV \geq 100 \text{ V}$
- ☑ $P_D \leq 312.5 \text{ W}$
- ☑ $I_D \leq 468 \text{ A}$
- ☑ $R_{DS(ON)} \leq 1.0 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate(G)	 Top View TO263-7L	
2, 3	Source(S)		
4	Drain(D)		
5, 6, 7	Source(S)		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_C=25^{\circ}\text{C}$	100	-	V
V_{GS}	Gate-Source Voltage	$T_C=25^{\circ}\text{C}$	-	± 20	V
$I_D^{*,***}$	Drain Current (DC)	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	468	A
		$T_C=100^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	330	A
$I_{DM}^{*,**}$	Drain Current (Pulsed)	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	1638	A
P_D	Power Dissipation	$T_C=25^{\circ}\text{C}$	-	312.5	W
E_{AS}	Single Pulsed Avalanche Energy	$V_{DD}=75\text{ V}, L=0.3\text{ mH}$	-	2535	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55	175	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		-	40	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case		-	0.48	$^{\circ}\text{C/W}$

Notes:

* Surface Mounted on 1 in² pad area, $t \leq 10\text{ sec}$.

** Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

*** Limited by bonding wire.

4. Marking Information

Product Name	Marking
KJ008N10D7	KJ008N10D7 HYWWZZ XXXXXX-X

5. Ordering Code

Product Name	Package	Reel size	Tape width	Quantity (pcs)
KJ008N10D7	TO263-7L	13"	24 mm	800

Note: KUAJIEXIN defines "Green" as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C).

6. Electrical Characteristics (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0 V, I _{DS} =250 μA	100	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250 μA	2.5	-	3.5	V
I _{DSS}	Drain Leakage Current	V _{DS} =100 V, V _{GS} =0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{DS} =0 V, V _{GS} =±20 V	-	-	±100	nA
R _{DS(ON)} ^a	On-State Resistance	V _{GS} =10 V, I _{DS} =50 A	-	0.8	1.0	mΩ
R _g	Gate Resistance		-	1	2	Ω
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	V _{GS} =0 V, I _{SD} =30 A	-	0.8	1.1	V
t _{rr}	Reverse Recovery Time	V _{DS} =50 V, V _{GS} =0 V, I _{DS} =30 A, di/dt=100 A/μs	-	110	-	ns
Q _{rr}	Reverse Recovery Charge		-	300	-	nC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{DS} =50 V, V _{GS} =0 V, f=1 MHz	-	11900	-	pF
C _{oss}	Output Capacitance		-	5400	-	
C _{rss}	Reverse Transfer Capacitance		-	250	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} =50 V, V _{GEN} =10 V, R _G =6 Ω, I _{DS} =30 A	-	55	-	ns
t _r	Turn-on Rise Time		-	100	-	
t _{d(off)}	Turn-off Delay Time		-	160	-	
t _f	Turn-off Fall Time		-	110	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} =50 V, V _{GS} =10 V, I _{DS} =30 A	-	180	-	nC
Q _{gs}	Gate-Source Charge		-	70	-	
Q _{gd}	Gate-Drain Charge		-	60	-	

Notes:

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

7. Typical Characteristics

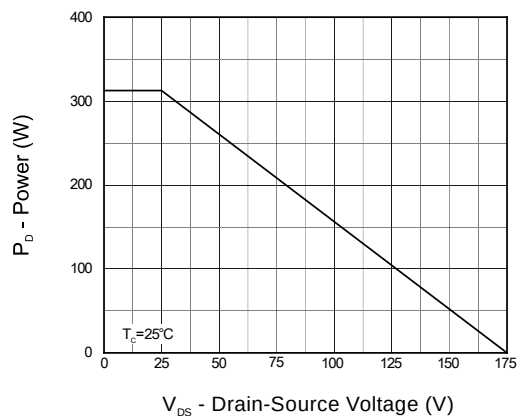


Fig 1. Output Characteristics

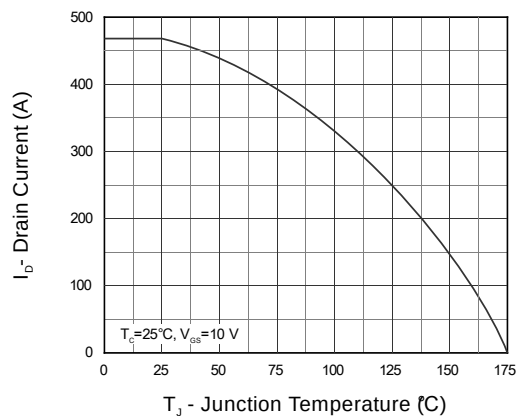


Fig 2. Current Capability

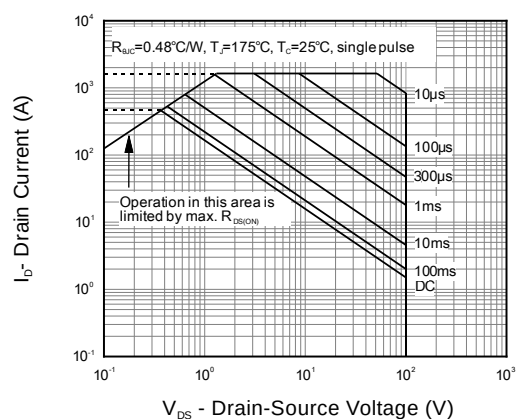


Fig 3. Safe Operation Area

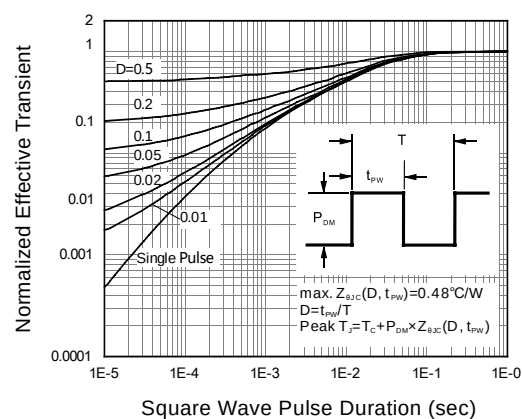


Fig 4. Transient Thermal Impedance

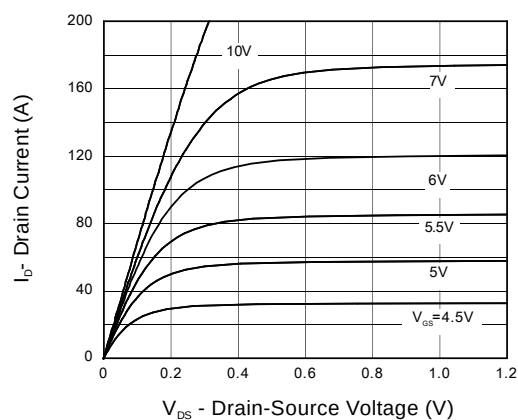


Fig 5. Output Characteristics

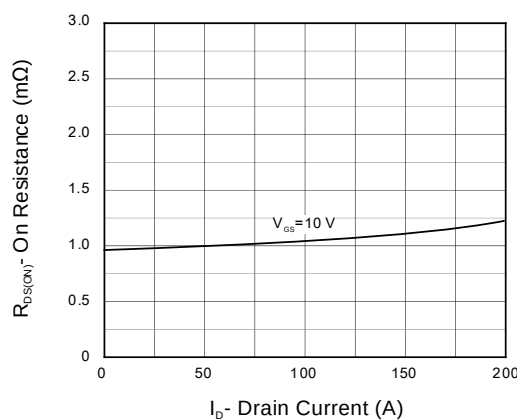


Fig 6. On Resistance

7. Typical Characteristics (cont.)

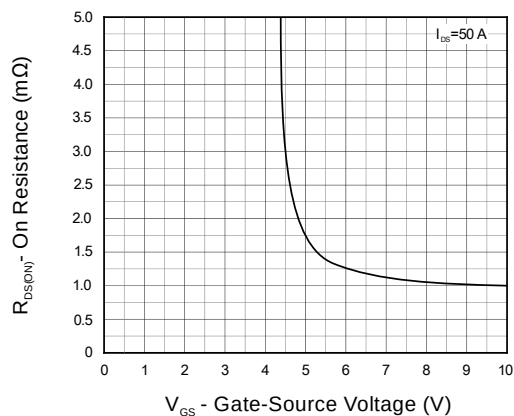


Fig 7. Transfer Characteristics

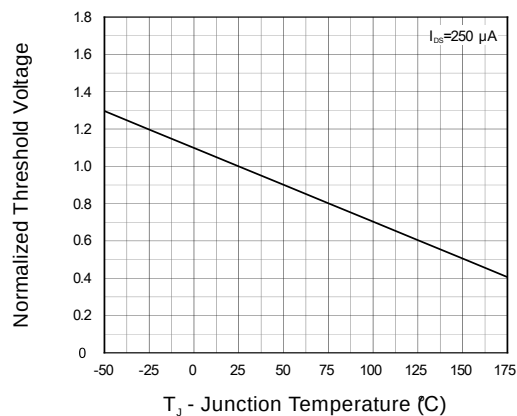


Fig 8. Normalized Threshold Voltage

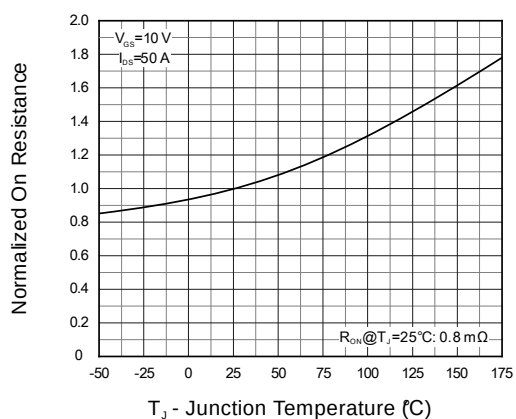


Fig 9. Normalized On Resistance

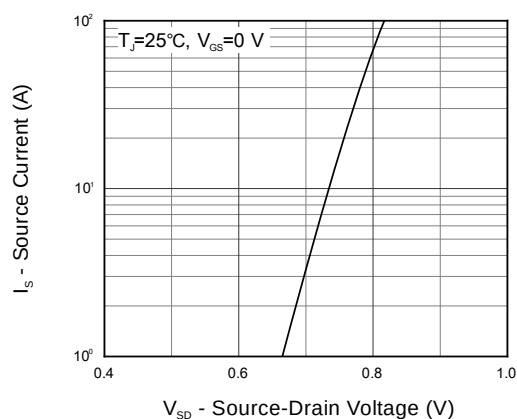


Fig 10. Diode Forward Current

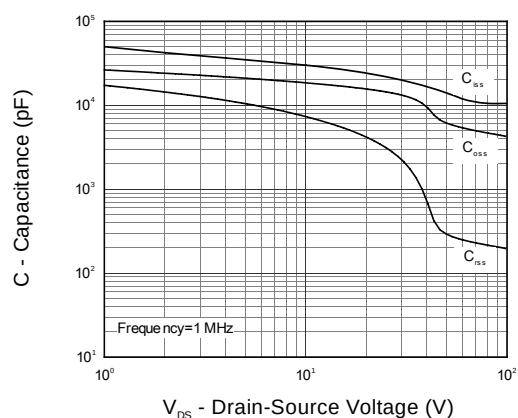


Fig 11. Capacitance

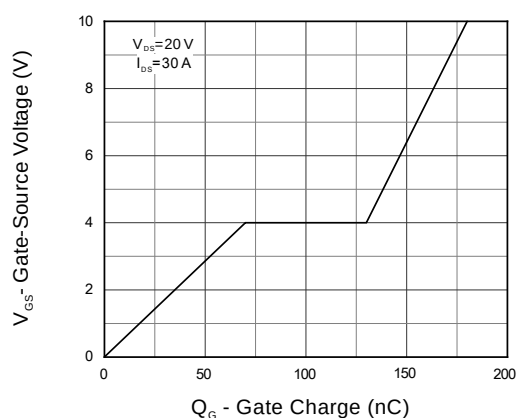
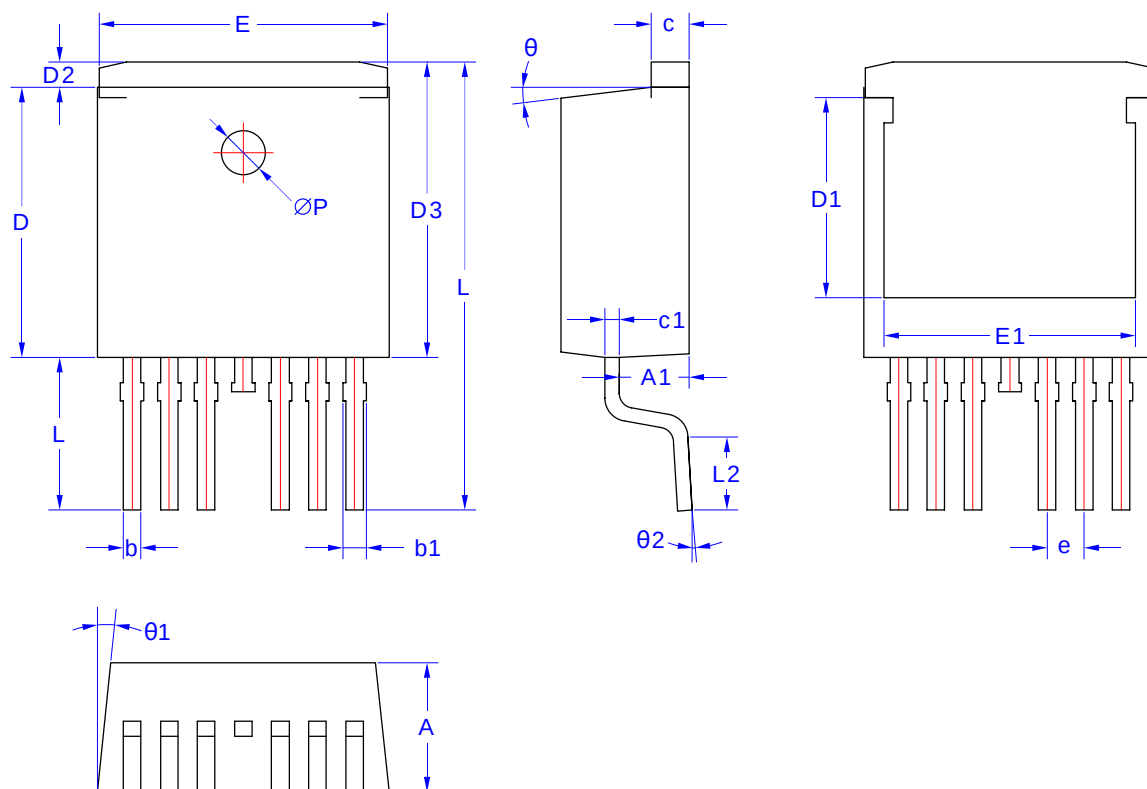


Fig 12. Gate Charge

8. Package Dimensions

TO263-7L Package



Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
A	4.20	4.40	4.60
A1	2.30	2.40	2.50
b	0.50	0.60	0.70
b1	0.60	0.70	0.80
c	1.25	1.30	1.35
c1	0.45	0.50	0.55
D	9.05	9.25	9.45
D1	6.65	6.85	7.05
D2	0.65	0.85	1.05
D3	9.90	10.10	10.30

Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
E	9.80	10.00	10.20
E1	8.50	8.60	8.70
e	-	1.27 BSC	-
L	14.90	15.10	15.40
L1	4.80	5.00	5.20
L2	2.30	2.50	2.70
θ	5°	7°	10°
$\theta 1$	3°	5°	8°
$\theta 2$	0°	-	8°
ΦP	-	1.50	-