

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☒ Advanced trench cell design
- ☒ Low thermal impedance
- ☒ Low gate charge

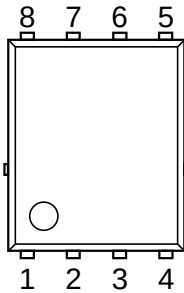
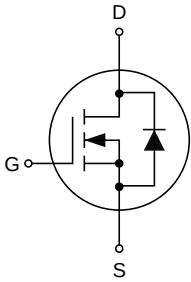
1.2 Applications

- ☒ DC/DC converter
- ☒ Power switch
- ☒ Motor drivers

1.3 Quick reference

- ☒ $BV \geq 100\text{ V}$
- ☒ $P_D \leq 104\text{ W}$
- ☒ $I_D \leq 100\text{ A}$
- ☒ $R_{DS(ON)} \leq 4.5\text{ m}\Omega @V_{GS} = 10\text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1,2,3	Source	 Top View PDFN5x6-8L	
4	Gate		
5,6,7,8	Drain		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_C=25^{\circ}\text{C}$	100	-	V
V_{GS}	Gate-Source Voltage	$T_C=25^{\circ}\text{C}$	-	± 20	V
I_D^*	Continuous Drain Current	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	100	A
		$T_C=100^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	79	A
I_{DM}^{***}	Pulsed Drain Current	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	400	A
P_D	Drain Power Dissipation	$T_C=25^{\circ}\text{C}$	-	104	W
E_{AS}	Single Pulsed Avalanche Energy	$V_{DD}=50\text{ V}, L=0.5\text{ mH}$	-	430	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55	150	$^{\circ}\text{C}$
$R_{\theta JA}^{**}$	Thermal Resistance-Junction to Ambient		-	58	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}^{**}$	Thermal Resistance-Junction to Case		-	1.2	

Notes:

- * Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- ** Surface mounted on 1 in^2 pad area, $t \leq 10\text{ sec}$.
- *** Pulse width limited by maximum junction temperature.

4. Marking Information

Product Name	Marking	
KJ045N10G	KJ045N10G YWWXXX YWWXXX: Date Code	

Ordering Code

Product Name	Package	Reel size	Tape width	Quantity (pcs)
KJ045N10G	PDFN 5x6-8L	13"	12 mm	5000

Note: KUIJIEXIN defines "Green" as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C).

6. Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0 V, I _{DS} =250 μA	100	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250 μA	2.4	-	3.6	V
I _{DSS}	Drain Leakage Current	V _{DS} =100 V, V _{GS} =0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{DS} =0 V, V _{GS} =±20 V	-	-	±100	nA
R _{DS(ON)} ^a	On-State Resistance	V _{GS} =10 V, I _{DS} =30 A	-	3.8	4.5	mΩ
g _{FS} ^b	Forward Transconductance	V _{GS} =5 V, I _{DS} =30 A	-	125	-	S
R _g	Gate Resistance	f=1 MHz	-	2.5	-	Ω
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	V _{GS} =0 V, I _{SD} =30 A	-	0.9	1.2	V
t _{rr}	Reverse Recovery Time	V _{DS} =50 V, I _{DS} =30 A,	-	50	-	ns
Q _{rr}	Reverse Recovery Charge	V _{GS} =0 V, dI _{SD} /dt=100 A/μs	-	108	-	nC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{DS} =50 V, V _{GS} =10 V, Frequency=1 MHz	-	4874	-	pF
C _{oss}	Output Capacitance		-	665	-	
C _{rss}	Reverse Transfer Capacitance		-	144	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} =50 V, V _{GEN} =10 V, R _G =6 Ω, I _{DS} =30 A	-	63	-	ns
t _r	Turn-on Rise Time		-	70	-	
t _{d(off)}	Turn-off Delay Time		-	86	-	
t _f	Turn-off Fall Time		-	41	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} =50 V, V _{GS} =10 V, I _{DS} =30 A	-	80	-	nC
Q _{gs}	Gate-Source Charge		-	22	-	
Q _{gd}	Gate-Drain Charge		-	25	-	

Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

7. Typical Characteristics

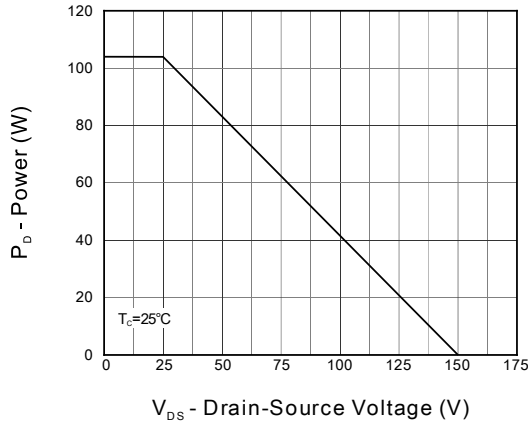


Figure 1. Output Characteristics

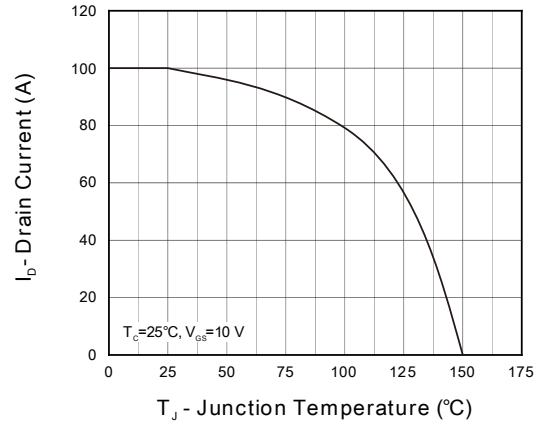


Figure 2. Current Capability

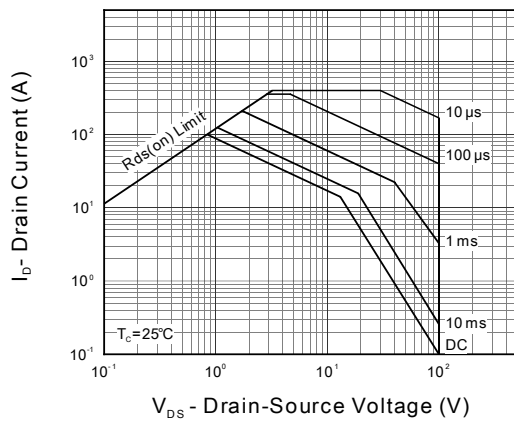


Figure 3. Safe Operation Area

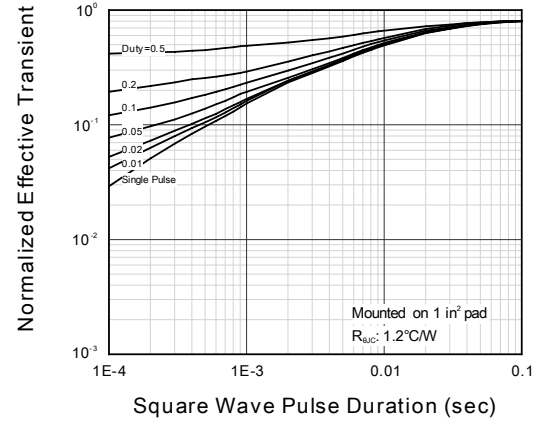


Figure 4. Transient Thermal Impedance

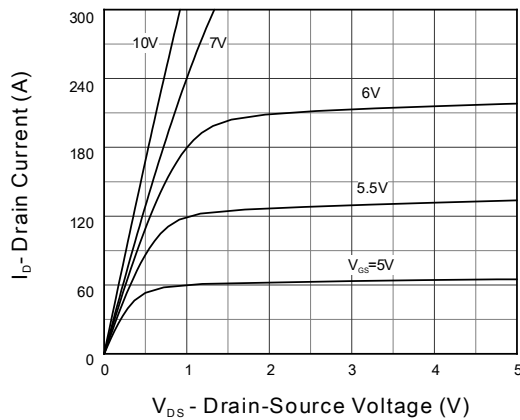


Figure 5. Output Characteristics

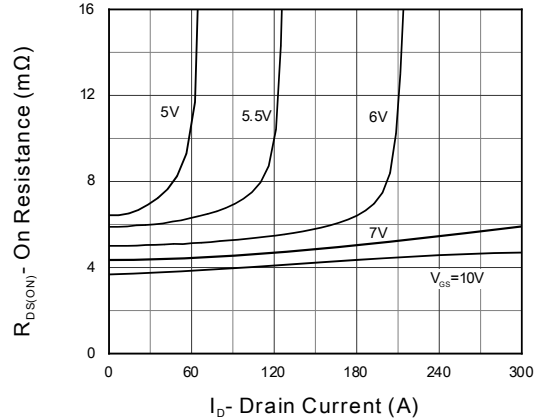


Figure 6. On Resistance

7. Typical Characteristics (cont.)

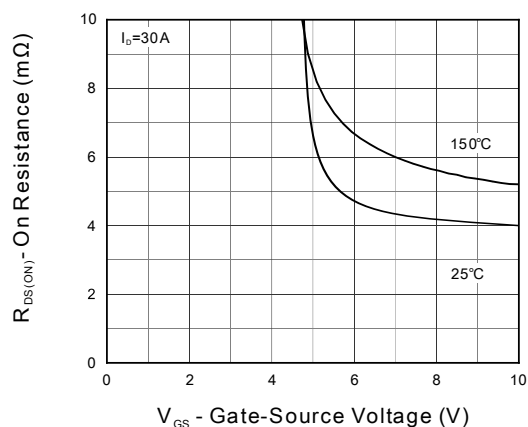


Figure 7. Transfer Characteristics

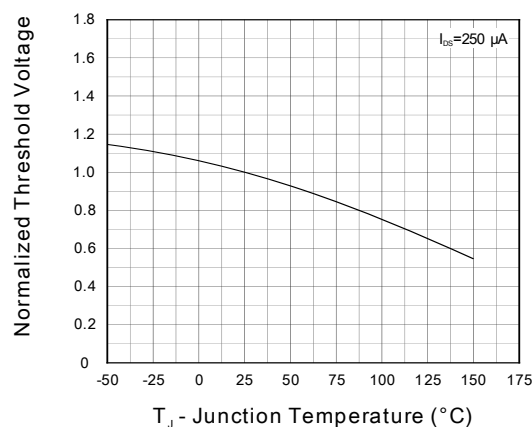


Figure 8. Normalized Threshold Voltage

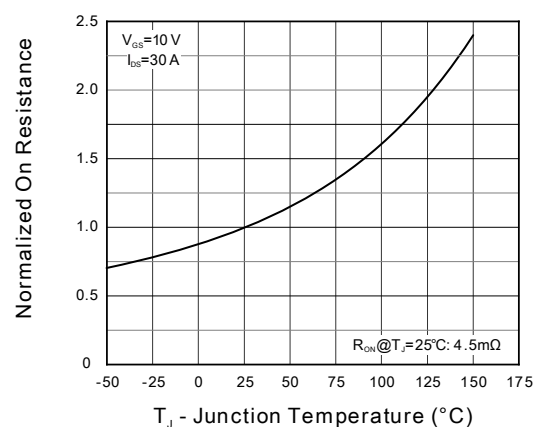


Figure 9. Normalized On Resistance

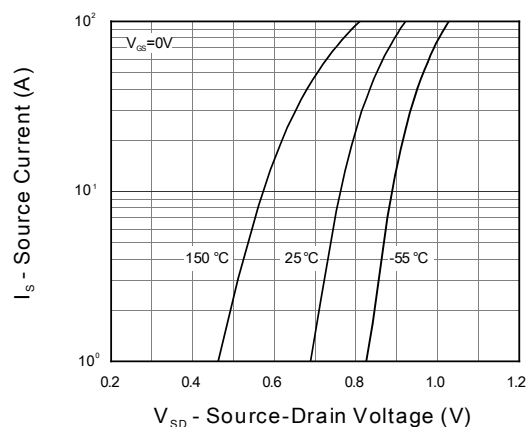


Figure 10. Diode Forward Current

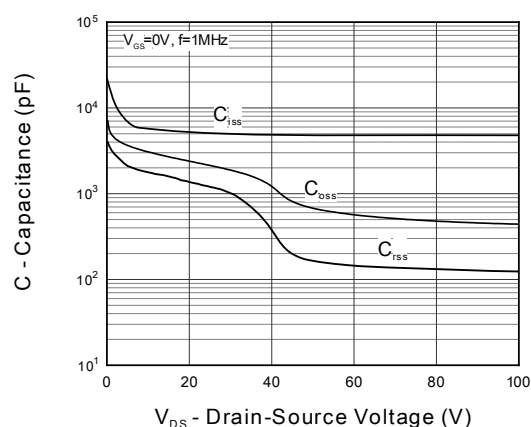


Figure 11. Capacitance

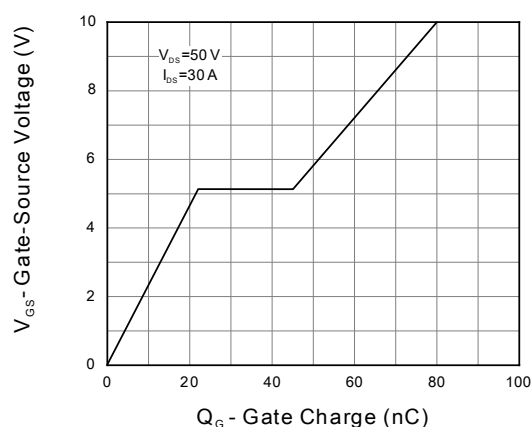
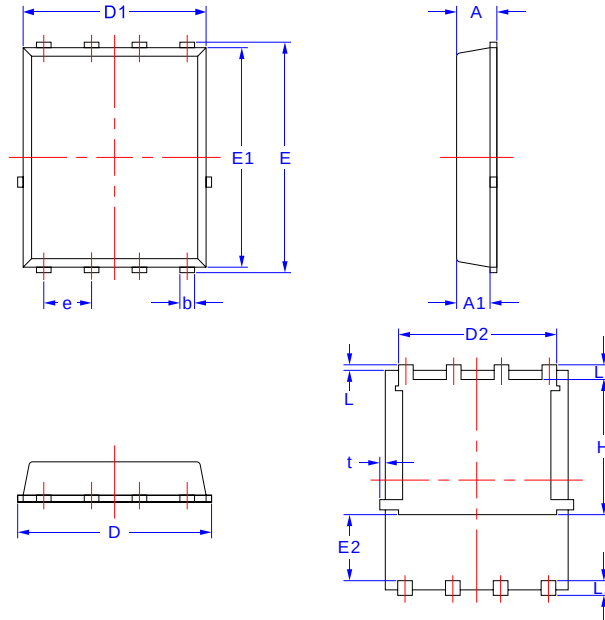


Figure 12. Gate Charge

8. Package Dimensions

PDFN 5x6-8L Package



Symbol	Dimensions in Millimeters	
	Min.	Max.
A	1.03	1.17
A1	0.82	0.97
b	0.34	0.48
D	4.80	5.40
D1	4.80	5.00
D2	4.11	4.31
E	5.95	6.15
E1	5.65	5.85
E2	1.60	-
e	1.270 BSC	
L	0.05	0.25
L1	0.38	0.50
L2	0.38	0.50
H	3.30	3.50
t	-	0.18