KJ1810QM

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Advanced trench cell design
- ☑ Low gate charge
- ☑ Low thermal impedance

1.2 Applications

- ☑ DC/DC converter
- ☑ Motor drivers
- ☑ Power switch
- ☑ Synchronous Rectification

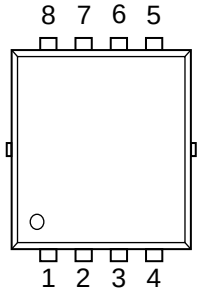
1.3 Quick reference

- ☑ BV ≥ 100 V
- ☑ P_D ≤ 68 W
- ☑ I_D ≤ 50 A
- ☑ $R_{DS(ON)}$ ≤ 18 mΩ @V_{GS} = 10 V

2. Pin Description

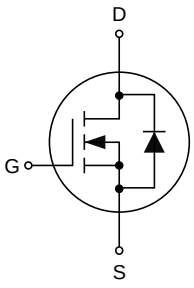
Pin	Description
1,2,3	Source
4	Gate
5,6,7,8	Drain

Simplified Outline



Top View
PDFN3.3x3.3-8L

Symbol



3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C=25℃	100	-	V
V_{GS}	Gate-Source Voltage	T_C=25℃	-	±20	V
I_D *	Continuous Drain Current	T_C=25℃, V_{GS}=10 V	-	50	A
		T_C=100℃, V_{GS}=10 V	-	31	A
I_{DM} ***	Pulsed Drain Current	T_C=25℃, V_{GS}=10 V	-	200	A
P_D	Drain Power Dissipation	T_C=25℃	-	68	W
E_{AS}	Single Pulsed Avalanche Energy	V_{DD}=50 V, L=0.5 mH	-	105	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55	150	℃
$R_{\theta JA}$ **	Thermal Resistance-Junction to Ambient		-	55	℃/W
$R_{\theta JC}$	Thermal Resistance-Junction to Case		-	1.85	

Notes:

* Pulse width ≤ 300 μs, duty cycle ≤ 2%.

** Surface mounted on 1 in^2 pad area, t ≤ 10 sec.

*** Pulse width limited by maximum junction temperature.

4. Marking Information

Product Name	Marking
KJ1810QM	**1810QM XXXXXX**

Ordering Code

Product Name	Package	Reel size	Tape width	Quantity (pcs)
KJ1810QM	**PDFN 3.3x3.3-8L**	**13"**	**12 mm**	**5000**

Note: KUAIJIEXIN defines “Green” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C).

6. Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0 V, I_{DS}=250 μA	100	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250 μA	1.2	1.8	2.5	V
I_{DSS}	Drain Leakage Current	V_{DS}=80 V, V_{GS}=0 V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{DS}=0 V, V_{GS}=±20 V	-	-	±100	nA
$R_{DS(ON)}$ [a]	On-State Resistance	V_{GS}=10 V, I_{DS}=20 A	-	16	18	mΩ
		V_{GS}=4.5 V, I_{DS}=10 A	-	21	25	mΩ
R_g	Gate Resistance	f=1 MHz	-	1.5	-	Ω
Diode Characteristics						
V_{SD} [a]	Diode Forward Voltage	V_{GS}=0 V, I_{SD}=20 A	-	0.9	1.0	V
t_{rr}	Reverse Recovery Time	V_{DS}=50 V, I_{DS}=20 A, V_{GS}=0 V, dI_{SD}/dt=100 A/μs	-	35	-	ns
Q_{rr}	Reverse Recovery Charge		-	32	-	nC
Dynamic Characteristics [b]						
C_{iss}	Input Capacitance	V_{DS}=25 V, V_{GS}=10 V, Frequency=1 MHz	-	1025	-	pF
C_{oss}	Output Capacitance		-	445	-	
C_{rss}	Reverse Transfer Capacitance		-	14	-	
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=50 V, V_{GEN}=10 V, R_G=3.3 Ω, I_{DS}=40 A	-	28	-	ns
t_r	Turn-on Rise Time		-	49	-	
$t_{d(off)}$	Turn-off Delay Time		-	226	-	
t_f	Turn-off Fall Time		-	93	-	
Gate Charge Characteristics [b]						
Q_g	Total Gate Charge	V_{DS}=50 V, V_{GS}=10 V, I_{DS}=40 A	-	80	-	nC
Q_{gs}	Gate-Source Charge		-	22	-	
Q_{gd}	Gate-Drain Charge		-	25	-	

Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

7. Typical Characteristics

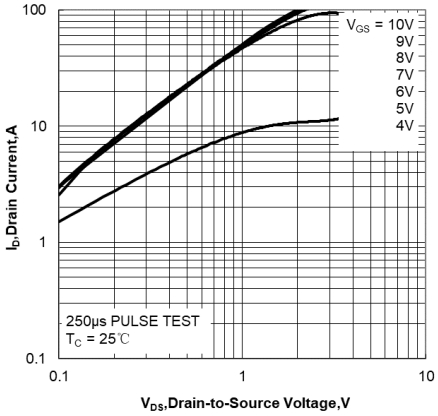


Figure 1. Output Characteristics

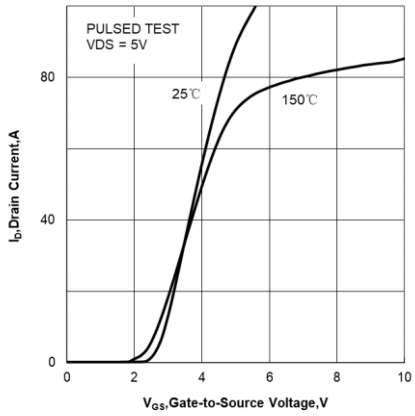


Figure 2. Transfer Characteristics

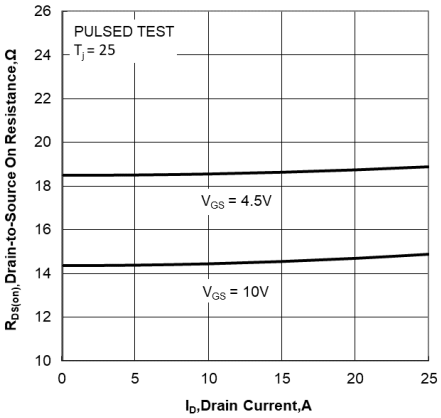


Figure 3. Drain-to-Source On Resistance vs Drain Current

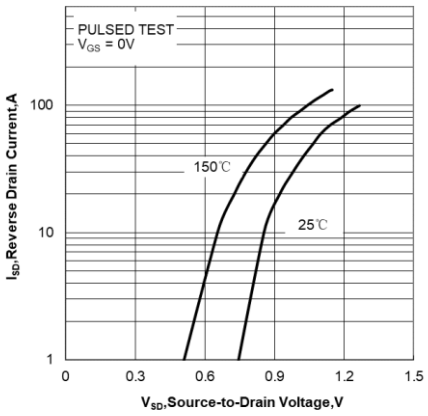


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

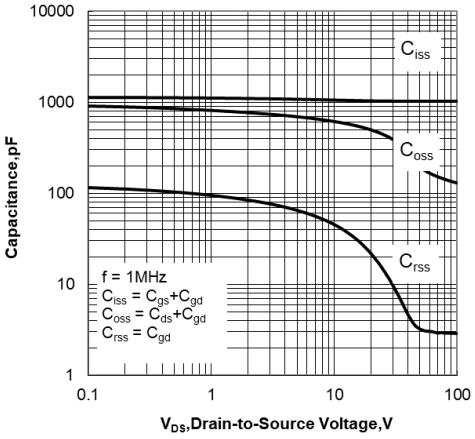


Figure 5. Capacitance Characteristics

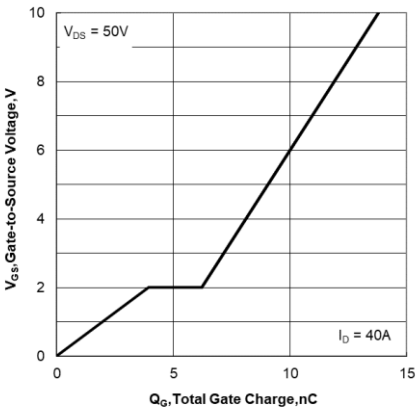


Figure 6. Gate Charge Characteristics

7. Typical Characteristics (cont.)

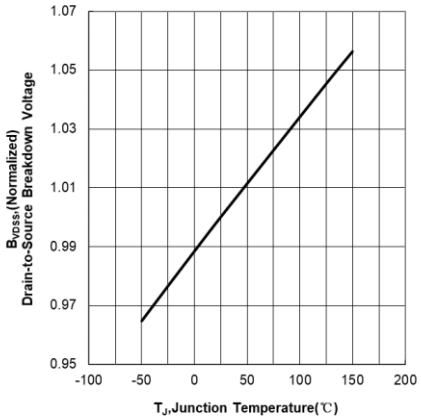


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

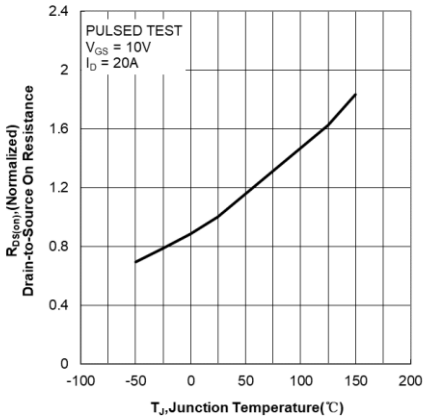


Figure 8. Normalized On Resistance vs Junction Temperature

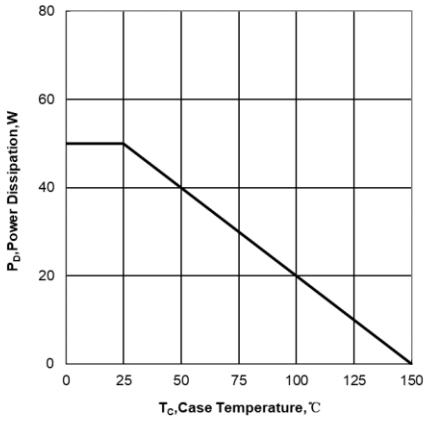


Figure 9. Maximum Continuous Drain Current vs Case Temperature

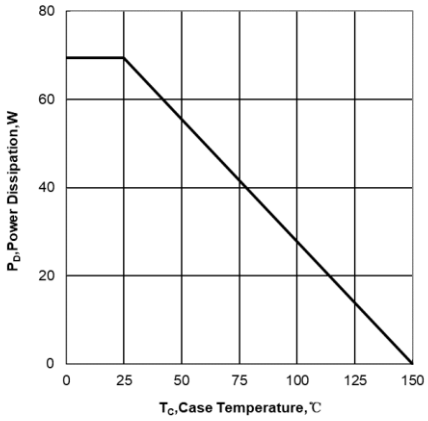


Figure 10. Maximum Power Dissipation vs Case Temperature

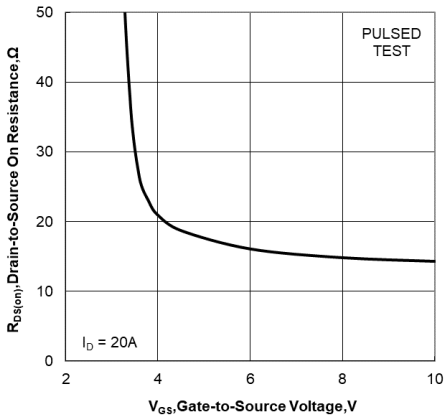


Figure11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

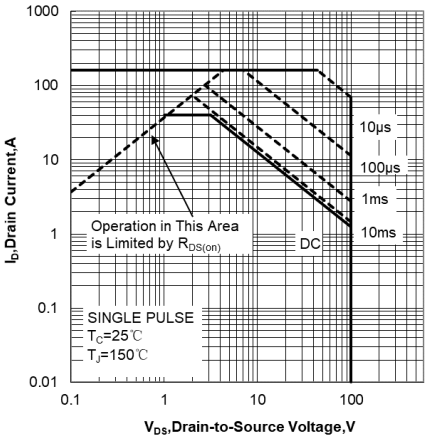
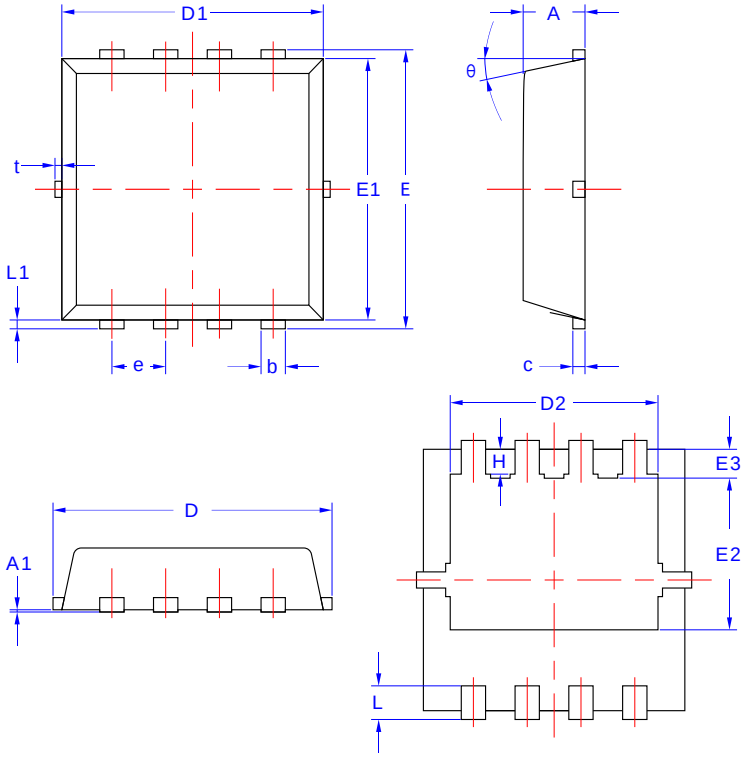


Figure 12. Maximum Safe Operating Area

8. Package Dimensions

PDFN 3.3x3.3-8L Package



Symbol	Dimensions in Millimeters	
	MIN	MAX
A	0.65	0.85
A1	/	0.05
b	0.20	0.40
c	0.10	0.25
D	3.15	3.45
D1	2.90	3.10
D2	2.30	2.60
E	3.15	3.45
E1	2.90	3.20
E2	1.54	1.94
E3	0.18	0.48
e	0.55	0.75
L	0.30	0.50
L1	0.06	0.20
H	0.31	0.52
t	0.00	0.13
θ	/	12°