

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☒ Advanced trench cell design
- ☒ Low Thermal Resistance

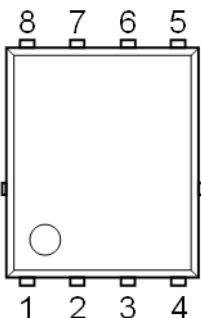
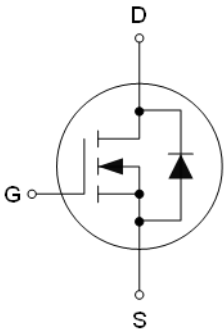
1.2 Applications

- ☒ Motor drivers
- ☒ DC - DC Converter

1.3 Quick reference

- ☒ $BV \geq 150\text{ V}$
- ☒ $P_{tot} \leq 50\text{ W}$
- ☒ $I_D \leq 40\text{ A}$
- ☒ $R_{DS(ON)} \leq 20\text{ m}\Omega @ V_{GS} = 10\text{ V}$
- ☒ $R_{DS(ON)} \leq 26\text{ m}\Omega @ V_{GS} = 6\text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1,2,3	Source	 Top View PDFN5x6-8L	
4	Gate		
5,6,7,8	Drain		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	Drain-Source Voltage	T _C =25°C	150	-	V
V _{GS}	Gate-Source Voltage	T _C =25°C	-	±20	V
I _D *	Drain Current (DC)	T _C =25°C, V _{GS} =10V	-	40	A
		T _C =100°C, V _{GS} =10V	-	25	A
I _{DM} **, **	Drain Current (Pulsed)	T _C =25°C, V _{GS} =10V	-	160	A
P _{tot} *	Total Power Dissipation	T _C =25°C	-	50	W
T _{stg}	Storage Temperature		-55	150	°C
T _J	Junction Temperature		-	150	°C
I _S	Diode Forward Current	T _C =25°C	-	40	A
E _{AS} *	Single Pulsed Avalanche Energy	V _{DD} =50 V, L=1.0 mH	-	50	mJ
R _{θJA} *	Thermal Resistance-Junction to Ambient		-	62.5	°C/W
R _{θJC} *	Thermal Resistance-Junction to Case		-	2.5	

Notes:

- * Surface mounted on 1 in² pad area, t ≤ 10 sec.
- ** Pulse width ≤ 300 μs, duty cycle ≤ 2%.
- *** Limited by bonding wire.

4. Marking Information

Product Name	Marking
KJ40N15G	40N15 XXXXXX

5. Ordering Code

Product Name	Package	Reel size	Tape width	Quantity (pcs)
KJ40N15G	PDFN 5x6-8L	13"	12 mm	5000

Note: KJ40N15G defines " Green " as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics (T_A=25°C unless otherwise noted)

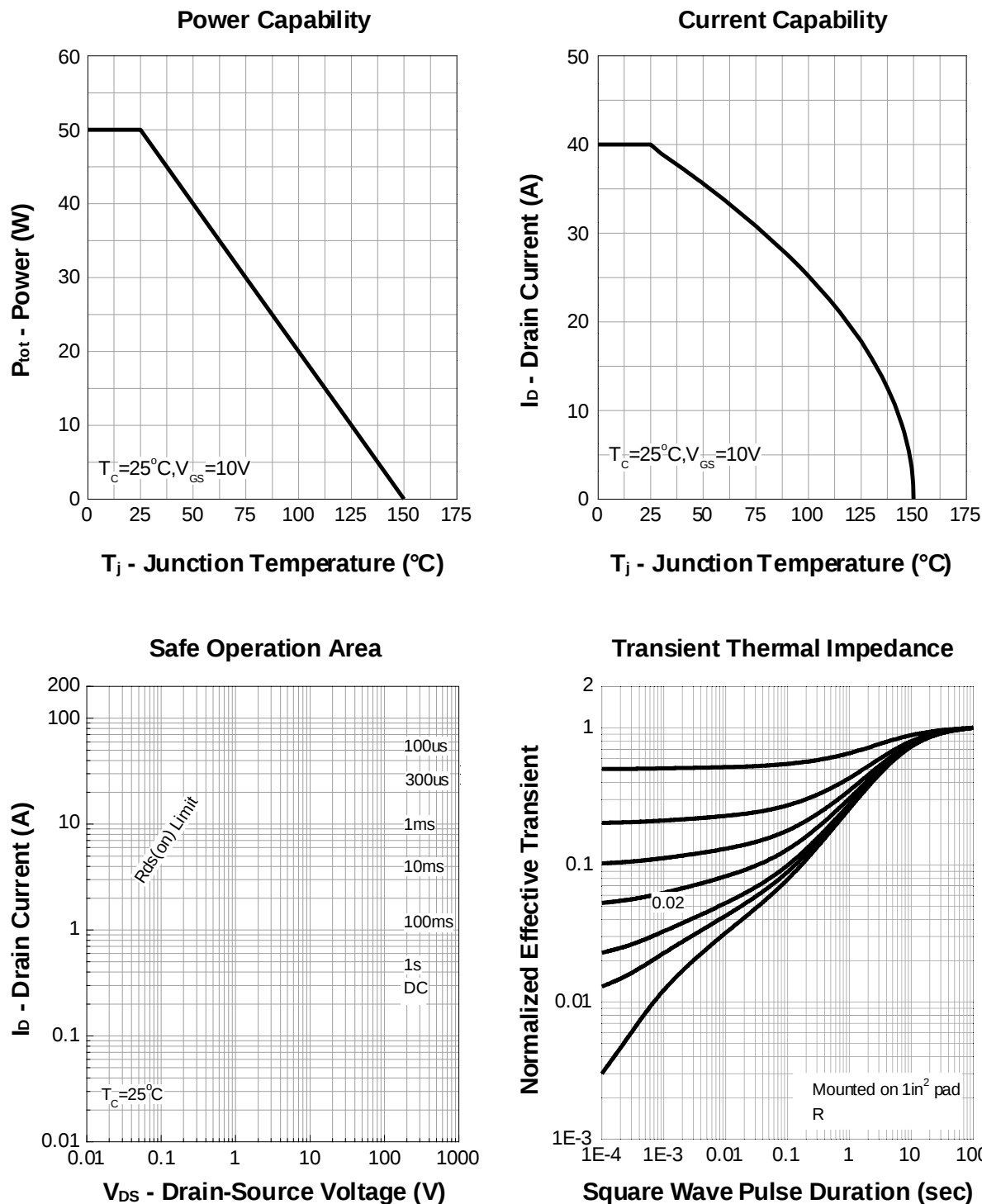
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0 V, I _D =250 μA	150	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250 μA	2	-	4	V
I _{DSS}	Zero Gate Voltage Source Current	V _{DS} =120 V, V _{GS} =0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{GS} =±20 V, V _{DS} =0 V	-	-	±100	nA
R _{DS(ON)} ^a	Drain-Source On-State Resistance	V _{GS} =10 V, I _D =15 A	-	15.5	20	mΩ
		V _{GS} =6 V, I _D =10 A	-	20.5	26	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} =15 A, V _{GS} =0 V	-	0.83	1.3	V
t _{rr}	Reverse Recovery Time	I _{SD} =15 A, dI _{SD} /dt=100 A/μs	-	72	-	ns
Q _{rr}	Reverse Recovery Charge		-	236	-	nC
Dynamic Characteristics ^b						
C _{iSS}	Input Capacitance	V _{GS} =0 V, V _{DS} =40 V Frequency=1 MHz	-	2450	-	pF
C _{oSS}	Output Capacitance		-	700	-	
C _{rSS}	Reverse Transfer Capacitance		-	38	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} =75 V, V _{GEN} =10 V, R _G =3.9 Ω, R _L =5 Ω, I _{DS} =15 A	-	10	-	ns
t _r	Turn-on Rise Time		-	12	-	
t _{d(off)}	Turn-off Delay Time		-	25	-	
t _f	Turn-off Fall Time		-	11	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} =75 V, V _{GS} =10 V, I _{DS} =15 A	-	35	-	nC
Q _{gs}	Gate-Source Charge		-	10	-	
Q _{gd}	Gate-Drain Charge		-	8	-	

Notes:

a. Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2%.

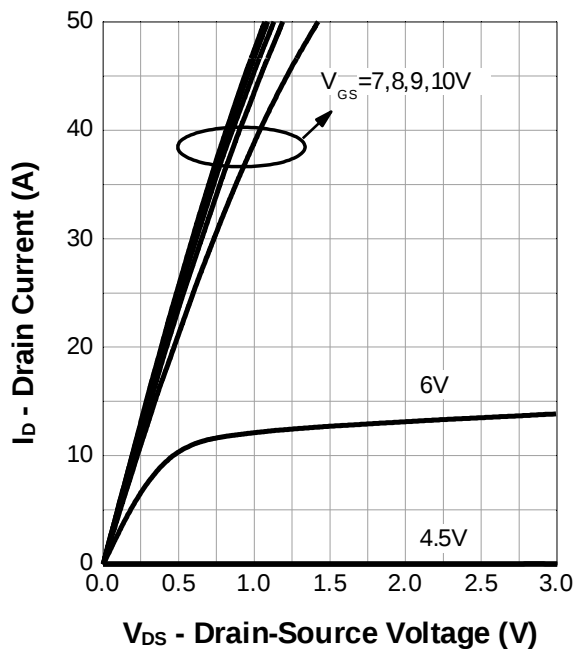
b. Guaranteed by design, not subject to production testing.

7. Typical Characteristics

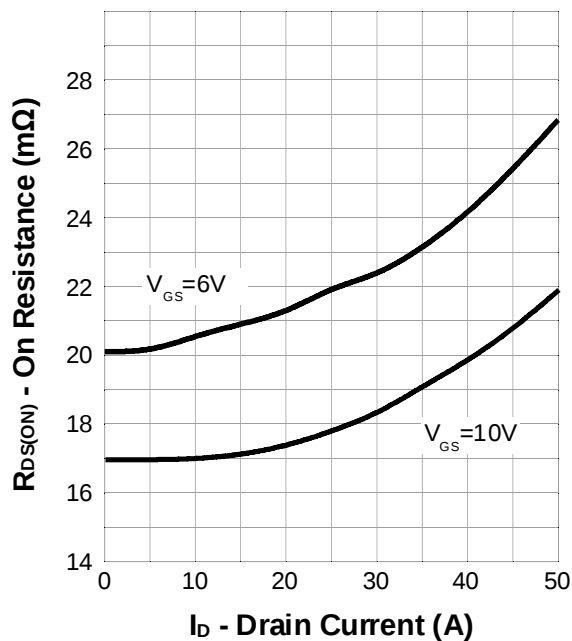


7. Typical Characteristics (cont.)

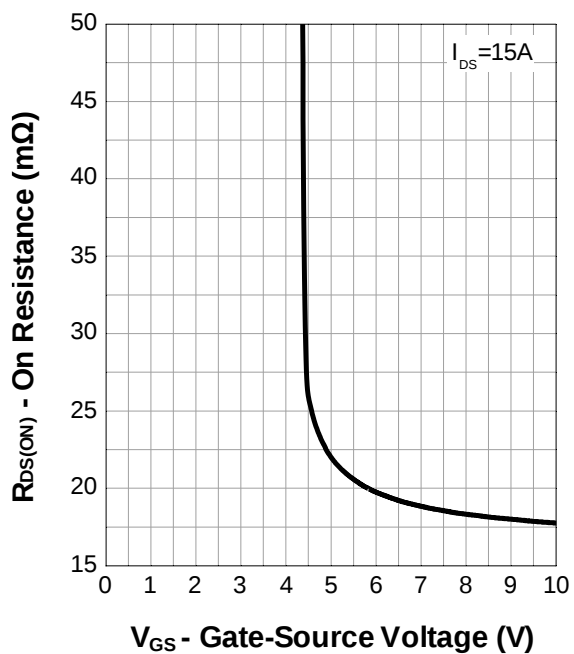
Output Characteristics



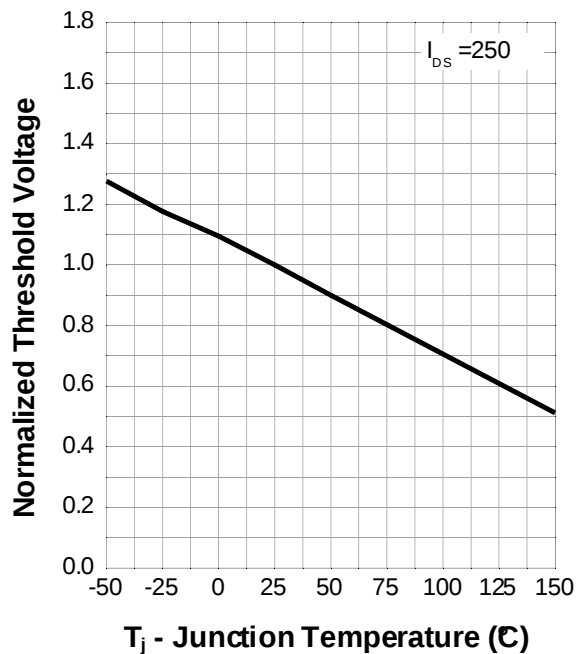
On Resistance



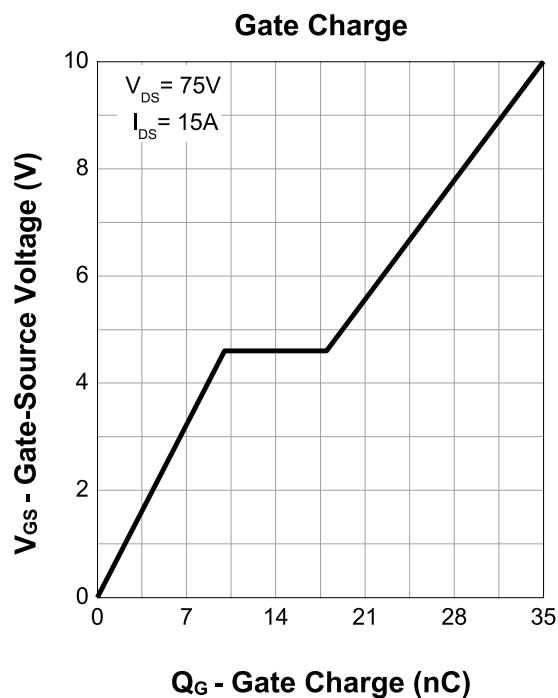
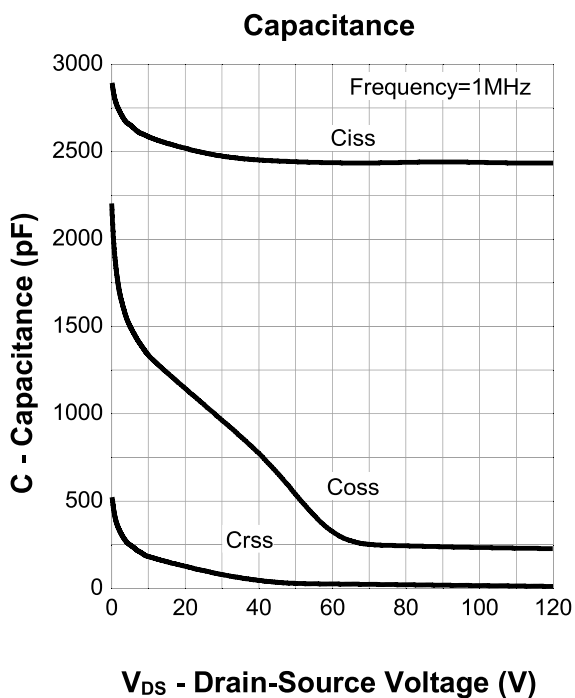
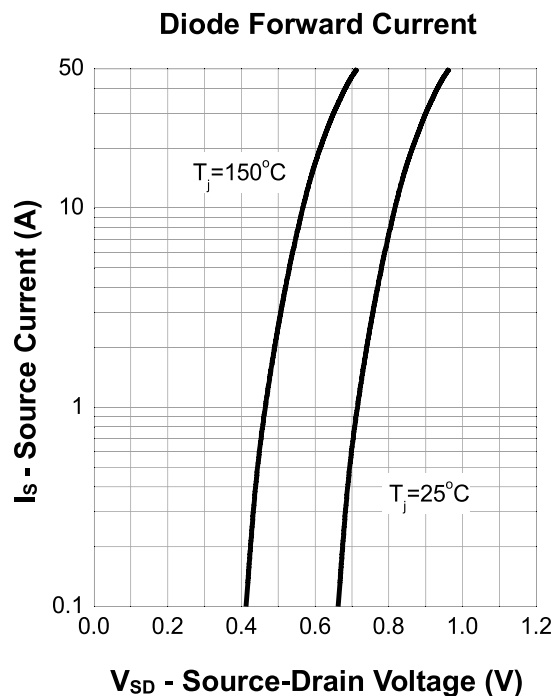
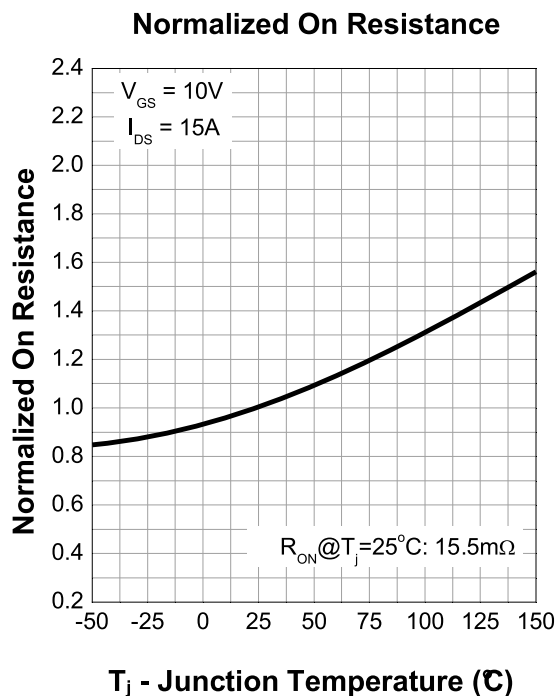
Transfer Characteristics



Normalized Threshold Voltage

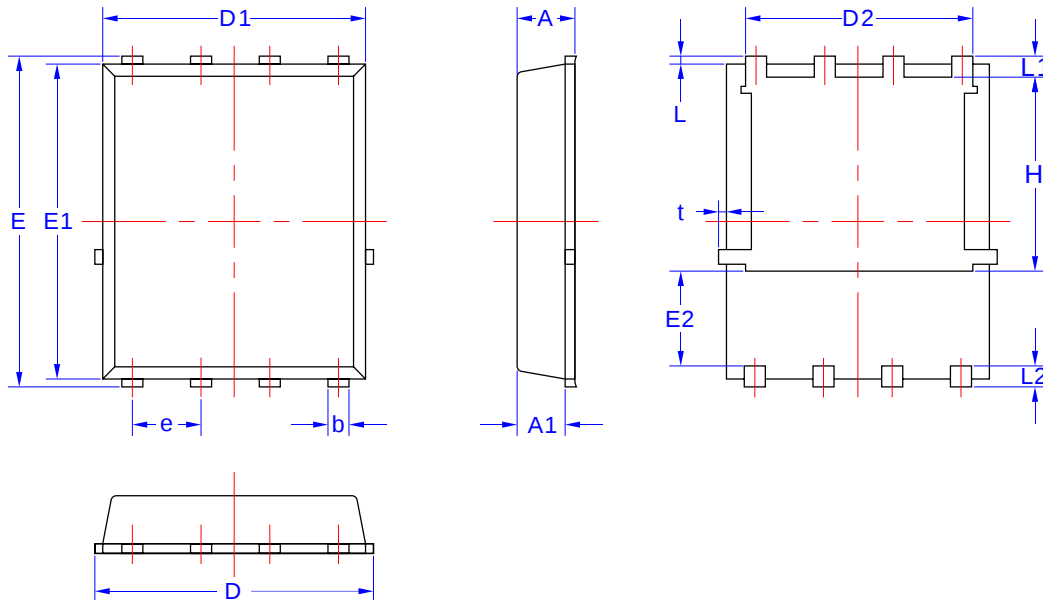


7. Typical Characteristics (cont.)



8. Package Dimensions

PDFN 5×6-8L Package



Symbol	Dimensions in Millimeters	
	MIN.	MAX
A	1.03	1.17
A1	0.824	0.97
b	0.34	0.48
D	4.80	5.40
D1	4.80	5.00
D2	4.11	4.31
E	5.95	6.15
E1	5.65	5.85
E2	1.40	-
e	1.27 BSC	
L	0.05	0.25
L1	0.38	0.50
L2	0.38	0.71
H	3.30	3.50
t	-	0.18