快捷芯
KUAIJIEXIN

KJ4P10DS

Dual P-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Surface-mounted package
- ☑ Low gate charge

1.2 Applications

- ☑ PWM applications
- ☑ Load switch

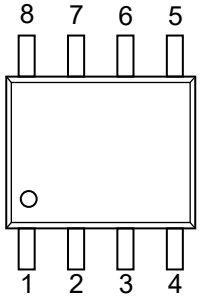
1.3 Quick reference

- ☑ BV ≤ -100 V
- ☑ P_D ≤ 2 W
- ☑ I_D ≤ -4 A
- ☑ $R_{DS(ON)}$ ≤ 150 mΩ @V_{GS} = -10 V
- ☑ $R_{DS(ON)}$ ≤ 180 mΩ @V_{GS} = -4.5 V

2. Pin Description

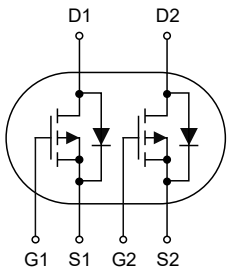
Pin	Description
1	Source 2
2	Gate 2
3	Source 1
4	Gate 1
5, 6	Drain 1
7, 8	Drain 2

Simplified Outline



Top View
SOP-8

Symbol



Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_A=25℃	-100	-	V
V_{GS}	Gate-Source Voltage	T_A=25℃	-	±20	V
I_D	Drain Current (DC)	T_A=25℃, V_{GS}=-10 V	-	-4	A
		T_A=70℃, V_{GS}=-10 V	-	-3.2	A
I_{DM} *	Drain Current (Pulsed)	T_A=25℃, V_{GS}=-10 V	-	-16	A
P_D	Drain Power Dissipation	T_A=25℃	-	2	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55	150	℃
$R_{\theta JA}$**	Thermal Resistance-Junction to Ambient		-	110	℃/W
$R_{\theta JC}$***	Thermal Resistance-Junction to Case		-	62.5	

Notes:

* Pulse width ≤ 300 μs, duty cycle ≤ 2%.

** Mounted on PCB of 1 in^2 pad area.

*** Mounted on large heat sink.

4. Marking Information

Product Name	Marking
KJ4P10DS	4P10DS YYXX YYXX: Date Code

5. Ordering Code

Product Name	Package	Reel size	Tape width	Quantity (pcs)
KJ4P10DS	SOP-8L	13"	12 mm	3000 or 4000

Note: KUAIJIEXIN defines “Green” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C).

6. Electrical Characteristics (T_C=25°C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0 V, I_{DS}=-250 μA	-100	-	-	V
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=-250 μA	-1.0	-1.8	-2.5	V
I_{DSS}	Drain Leakage Current	V_{DS}=-100 V, V_{GS}=0 V	-	-	-1.0	μA
I_{GSS}	Gate Leakage Current	V_{DS}=0 V, V_{GS}=±20 V	-	-	±100	nA
$R_{DS(ON)}$[a]	On-State Resistance	V_{GS}=-10 V, I_{DS}=-4 A	-	105	150	mΩ
		V_{GS}=-4.5 V, I_{DS}=-3 A	-	110	180	
Diode Characteristics						
V_{SD} [a]	Diode Forward Voltage	I_{SD}=-2 A, V_{GS}=0 V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	I_{SD}=-2 A, dI_{SD}/dt=100 A/μs	-	70	-	ns
Q_{rr}	Reverse Recovery Charge		-	215	-	nC
Dynamic Characteristics [b]						
C_{iss}	Input Capacitance	V_{GS}=0 V, V_{DS}=-50 V, Frequency=1MHz	-	1050	-	pF
C_{oss}	Output Capacitance		-	61	-	
C_{rss}	Reverse Transfer Capacitance		-	38	-	
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=-50 V, V_{GEN}=-10 V, R_G=3 Ω, I_{DS}=-4 A	-	8	-	ns
t_r	Turn-on Rise Time		-	15	-	
$t_{d(off)}$	Turn-off Delay Time		-	68	-	
t_f	Turn-off Fall Time		-	22	-	
Gate Charge Characteristics [b]						
Q_g	Total Gate Charge	V_{DS}=-50 V, V_{GS}=-10 V, I_{DS}=-2 A	-	18	-	nC
Q_{gs}	Gate-Source Charge		-	5	-	
Q_{gd}	Gate-Drain Charge		-	6	-	

Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

7. Typical Characteristics

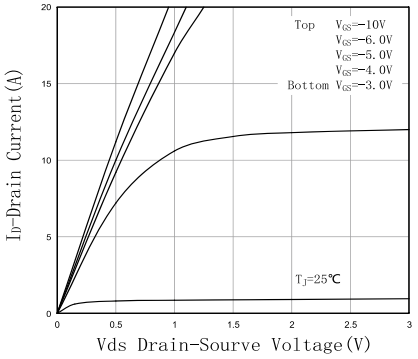


Fig.1 Output Characteristic

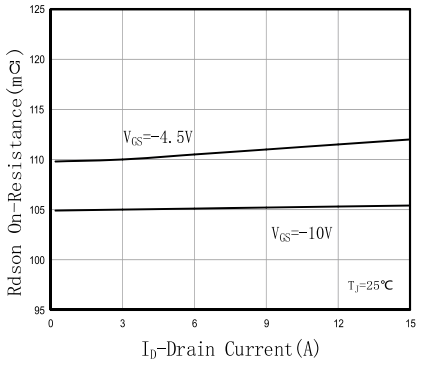


Fig.2 On-Resistance vs. Drain Current

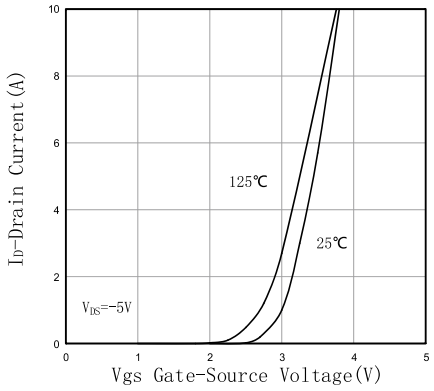


Fig.3 Transfer Characteristic

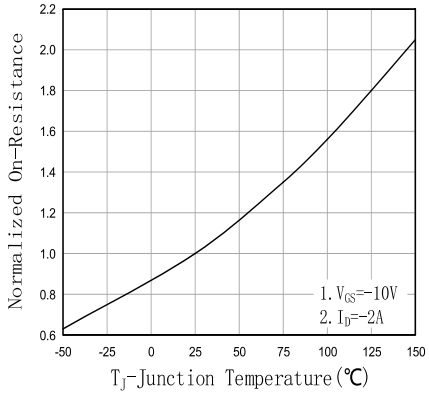


Fig.4 On-Resistance vs. Junction Temperature

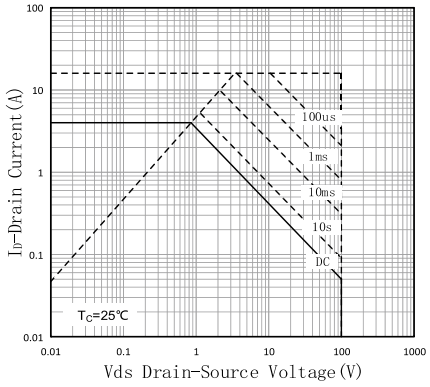


Fig.5 Safe Operation Area

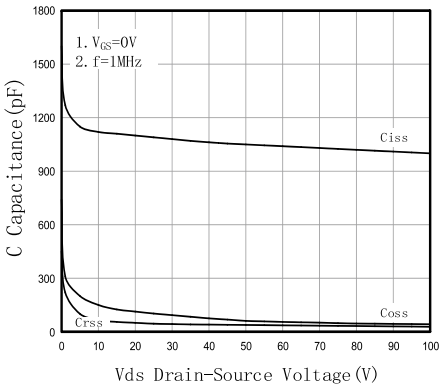


Fig.6 Capacitance Characteristic

7. Typical Characteristics (cont.)

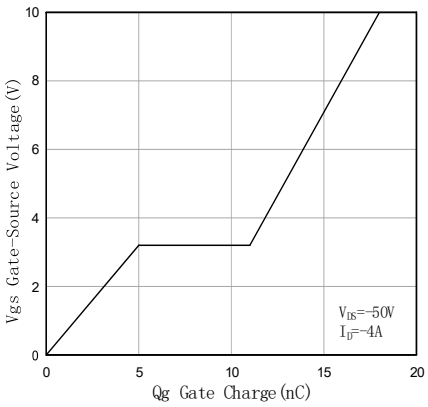


Fig.7 Gate-Charge Characteristic

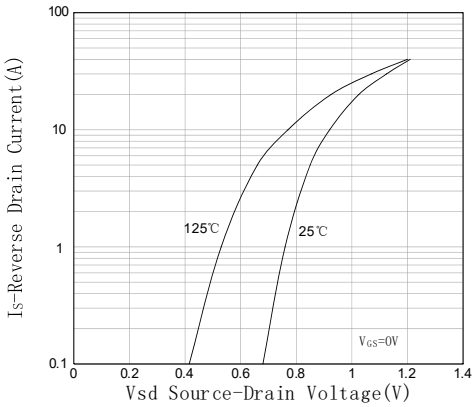
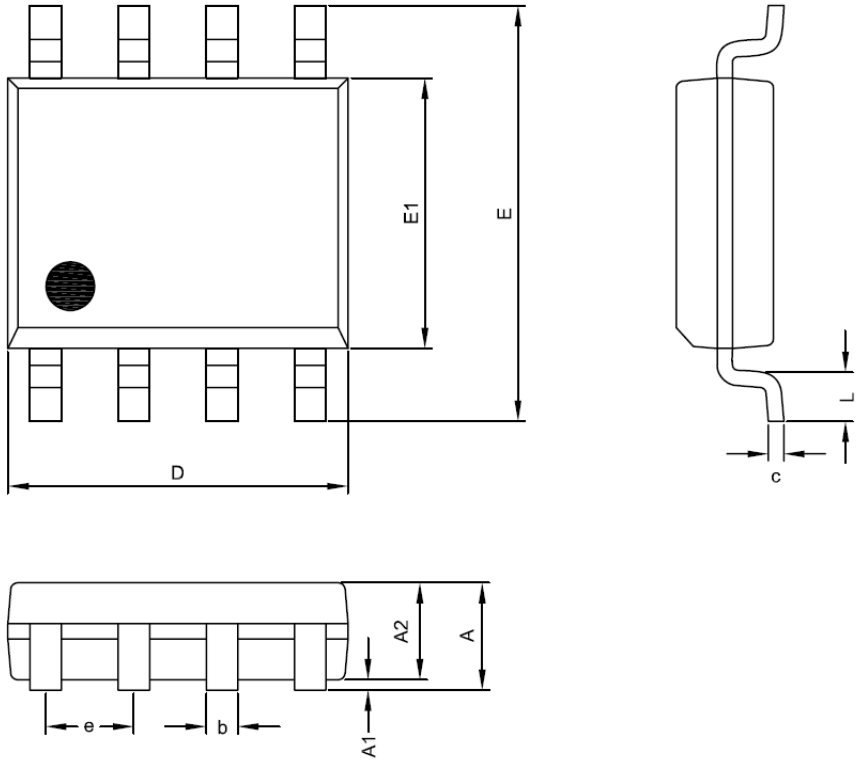


Fig.8 Body Diode Characteristic

8. Package Dimensions

SOP-8L Package



Symbol	Dimensions in Millimeters	
	MIN	MAX
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.90	5.10
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27