KJ4668P

N-Channel Enhancement Mode MOSFET

1. Product Information

Features

Advanced trench Technology

Excellent $R_{DS(ON)}$ and Switching Performance

Applications

UPS

Inverter

Quick reference

V_{DS} = 200 V

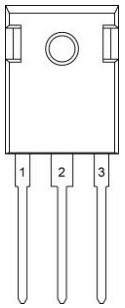
I_D = 150 A

$R_{DS(ON)}$ ≦ 10 mΩ @ V_{GS}=10 V（Type: 8.5 mΩ）

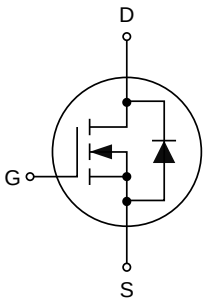
Pin Description

Pin	Description
1	Gate(G)
2	Drain(D)
3	Source(S)

Simplified Outline	Symbol



Top View
TO-247-3L



Package Marking and Ordering Information

Product Name	Package	Marking	Reel Size	Tape Width	Quantity
KJ4668P	**TO-247-3L**	**KJ4668 XXXYYY**	**-**	**-**	**300**

2. Absolute Maximum Ratings (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Values	Unit
V_{DS}	Drain-Source Voltage	200	V
V_{GS}	Gate-Source Voltage	±30	V
I_D	Continuous Drain Current, V_{GS}@10 V, T_C=25℃	150	A
	Continuous Drain Current, V_{GS}@10 V, T_C=100℃	102	A
I_{DM}	Pulsed Drain Current	450	A
E_{AS}	Single Pulse Avalanche Energy	600	mJ
E_{AR}	Avalanche Energy, Repetitive	150	mJ
I_{AS}	Avalanche Current	90	A
dv/dt	Peak Diode Recovery dv/dt	10.0	V/ns
P_D	Power Dissipation, T_C=25℃ [4]	750	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55~150	℃
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	40	℃/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.45	℃/W

3. Electrical Characteristics (T_J=25℃, unless otherwise noted)

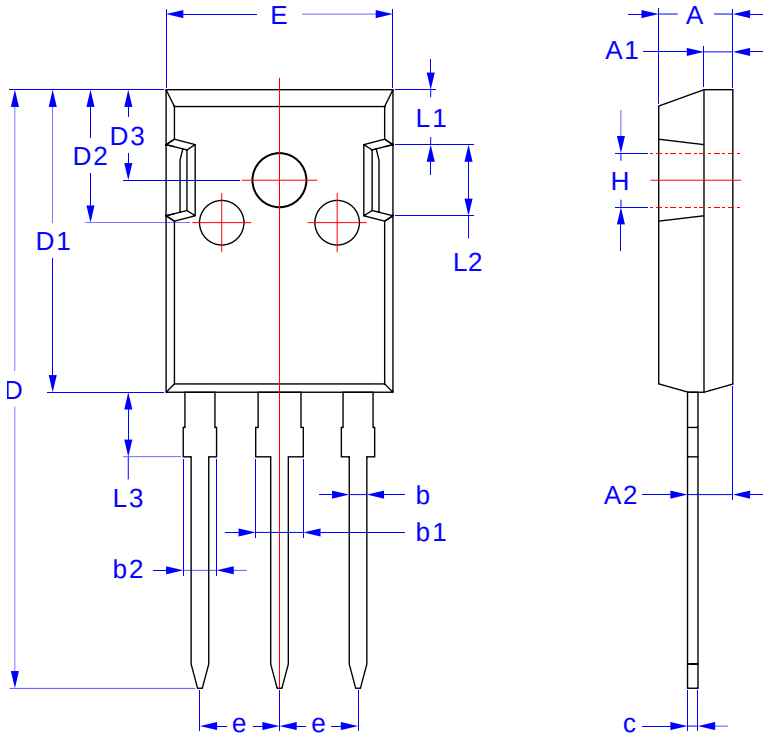
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0 V, I_D=250 μA	200	220	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=200 V, V_{GS}=0 V, T_C=25℃	-	-	1.0	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=200 V, V_{GS}=0 V, T_C=125℃	-	-	100	μA
I_{GSS}	Gate-body Leakage current	V_{DS}=0 V, V_{GS}=±20 V	-	-	±100	nA
$V_{GS(th)}$	Gate-Threshold Voltage	V_{DS}=V_{GS}, I_D=250 μA	3.6	4.3	5.0	V
$R_{DS(on)}$	Drain-Source on-Resistance	V_{GS}=10 V, I_D=80 A	-	8.5	10	mΩ
gfs	Forward Trans conductance	V_{DS}=25 V, I_D=80 A	50	65	-	S
R_g	Total Gate Charge	V_{GS}=0 V, V_{DS}=0 V, f=1 MHz	-	1.3	-	Ω
C_{iss}	Input Capacitance	V_{DS}=50 V, V_{GS}=0 V, f=1 MHz	-	15000	-	pF
C_{oss}	Output Capacitance		-	1000	-	
C_{rss}	Reverse Transfer Capacitance		-	420	-	
$t_{d(on)}$	Turn-on Delay Time	V_{GS}=10 V, V_{DS}=50 V, R_G=2.5 Ω, I_D=80 A	-	90	-	ns
t_r	Turn-on Rise Time		-	140	-	
$t_{d(off)}$	Turn-off Delay Time		-	220	-	
t_f	Turn-off Fall Time		-	180	-	
Q_g	Total Gate Charge	V_{GS}=10 V, V_{DS}=100 V, I_D=80 A	-	170	-	nC
Q_{gs}	Gate-Source Charge		-	30	-	
Q_{gd}	Gate-Drain Charge		-	50	-	
V_{SD}	Diode Forward Voltage	I_S=80 A, V_{GS}=0 V	-	-	1.2	V
I_S	Continuous Source Current (Body Diode)		-	-	150	A
I_{SM}	Maximum Pulsed Current (Body Diode)		-	-	500	A
t_{rr}	Reverse Recovery Time	I_S=60 A, V_{DD}=50 V, dI/dt=100 A/μs	-	220	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.1	-	nC

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2 OZ copper.
2. The data tested by pulsed, pulse width ≤ 300 μs, duty cycle ≤ 2%
3. The E_{AS} data shows Max. rating. The test condition is T_J=25℃, L=0.3 mH, R_G=25 Ω, V_{DD}=50 V, V_{GS}=10 V
4. The I_S=80 A, di/dt ≤ 100 A/us, V_{DD} ≤ V_{DS}, Start T_J=25℃
5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

4. Package Mechanical Data

TO-247-3L



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	4.90	5.10
A1	1.90	2.10
A2	2.00	3.00
b	0.55	0.75
b1	2.50	3.50
b2	1.75	2.50
c	1.20	1.30
D	41.00	42.00
D1	20.00	21.00
D2	8.00	10.00
D3	5.00	6.00
E	15.00	16.00
e	TYP 5.08	
H	3.00	3.50
L1	3.50	4.00
L2	4.75	5.25
L3	4.00	5.00