

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☒ Surface-mounted package
- ☒ 100% Avalanche Tested
- ☒ $T_{J\max}$ 175°C
- ☒ Advanced trench cell design
- ☒ 100% DVDS Tested
- ☒ MSL1

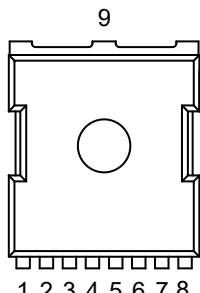
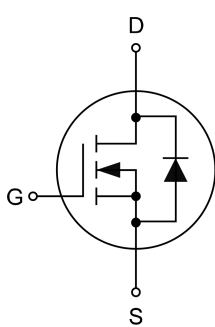
1.2 Applications

- ☒ DC/DC Conversion
- ☒ Motor Drives
- ☒ Power Switch
- ☒ Battery management

1.3 Quick reference

- ☒ $BV \geq 100\text{ V}$
- ☒ $P_D \leq 326\text{ W}$
- ☒ $I_D \leq 289\text{ A}$
- ☒ $R_{DS(ON)} \leq 1.8\text{ m}\Omega @V_{GS} = 10\text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate	 Top View TOLL-8L	
2,3,4,5,6,7,8	Source		
9	Drain		

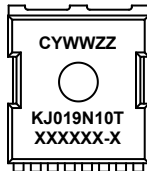
3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_C=25^{\circ}\text{C}$	100	-	V
V_{GS}	Gate-Source Voltage	$T_C=25^{\circ}\text{C}$	-	± 20	V
I_D	Drain Current (DC)	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	289	A
		$T_C=100^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	204	A
I_{DM}^*	Drain Current (Pulsed)	$T_C=25^{\circ}\text{C}, V_{GS}=10\text{ V}$	-	1156	A
P_D	Drain power dissipation	$T_C=25^{\circ}\text{C}$	-	326	W
E_{AS}	Single Pulsed Avalanche Energy	$V_{DD}=50\text{ V}, L=0.3\text{ mH}$	-	1452	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55	175	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		-	45	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case		-	0.46	

Notes:

- * Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- ** Surface mounted on 1 in^2 pad area, $t \leq 10\text{ sec.}$
- *** Limited by bonding wire.

4. Marking Information

Product Name	Marking
KJ019N10T	

5. Ordering Code

Product Name	Package	Reel size	Tape width	Quantity (pcs)
KJ019N10T	TOLL-8L	13"	24 mm	2000

Note: KUAJIEXIN defines "Green" as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C)

6. Electrical Characteristics (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0 V, I _{DS} =250 μA	100	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250 μA	2	-	4	V
I _{DSS}	Drain Leakage Current	V _{DS} =80 V, V _{GS} =0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{DS} =0 V, V _{GS} =±20 V	-	-	±100	nA
R _{DS(ON)}	On-State Resistance	V _{GS} =10 V, I _{DS} =50 A	-	1.55	1.8	mΩ
R _g	Gate Resistance	Frequency=1 MHz	-	1.5	-	Ω
Diode Characteristics						
V _{SD}	Diode Forward Voltage	V _{GS} =0 V, I _{SD} =50 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} =0 V, I _{DS} =50 A, dI _{SD} /dt=100 A/μs	-	104	-	ns
Q _{rr}	Reverse Recovery Charge		-	285	-	nC
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =50 V, V _{GS} =0 V, Frequency=1 MHz	-	10200	-	pF
C _{oss}	Output Capacitance		-	1320	-	
C _{rss}	Reverse Transfer Capacitance		-	67	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} =50 V, V _{GEN} =10 V, R _G =2 Ω, R _L =1 Ω, I _{DS} =50 A	-	36	-	ns
t _r	Turn-on Rise Time		-	30	-	
t _{d(off)}	Turn-off Delay Time		-	82	-	
t _f	Turn-off Fall Time		-	30	-	
Gate Charge Characteristics						
Q _g	Total Gate Charge	V _{DS} =50 V, V _{GS} =10 V, I _{DS} =50 A	-	195	-	nC
Q _{gs}	Gate-Source Charge		-	53	-	
Q _{gd}	Gate-Drain Charge		-	56	-	

7. Typical Characteristics

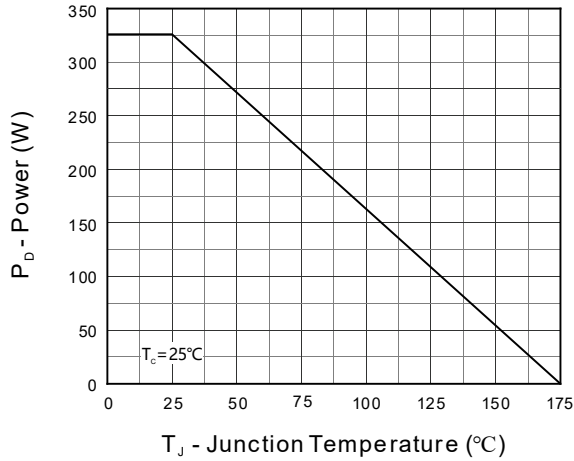


Figure 1. Power Capability

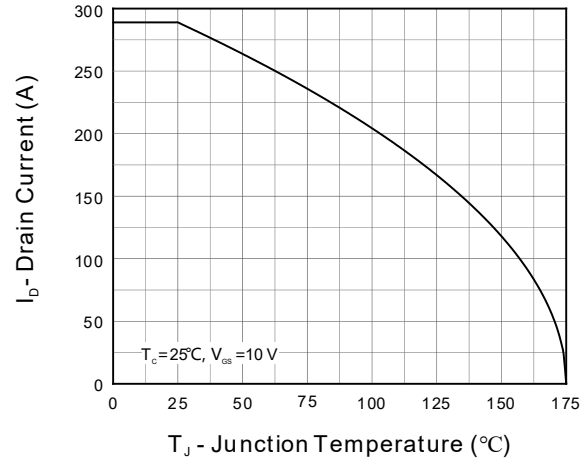


Figure 2. Current Capability

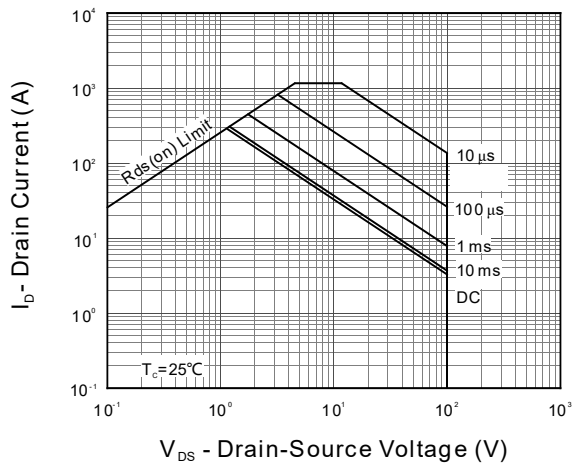


Figure 3. Safe Operation Area

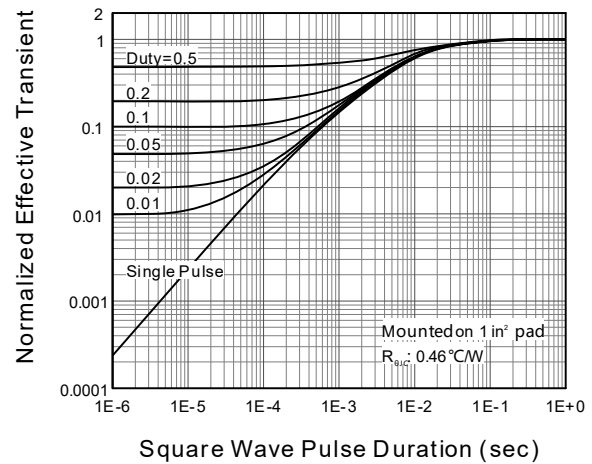


Figure 4. Transient Thermal Impedance

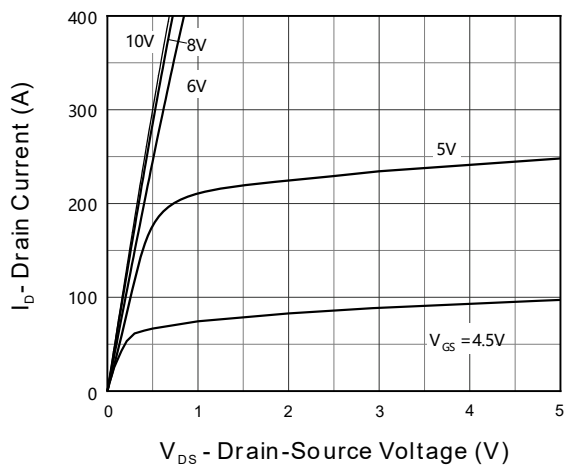


Figure 5. Output Characteristics

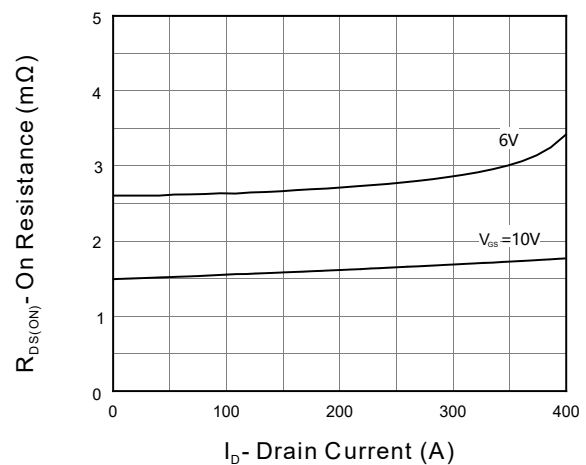


Figure 6. On Resistance

7. Typical Characteristics (cont.)

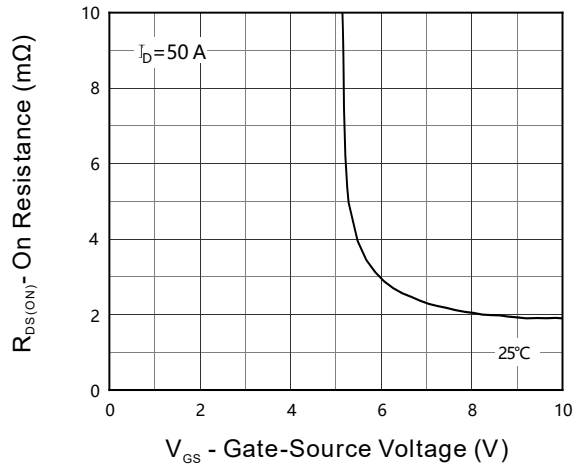


Figure 7. Transfer Characteristics

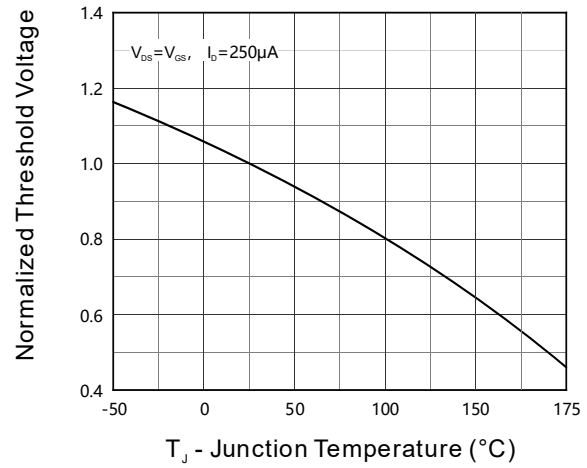


Figure 8. Normalized Threshold Voltage

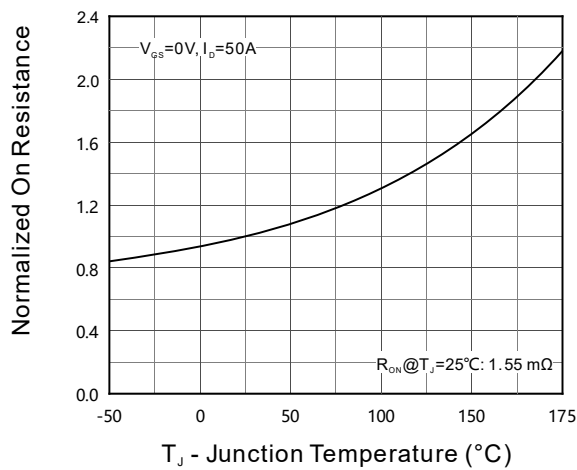


Figure 9. Normalized On Resistance

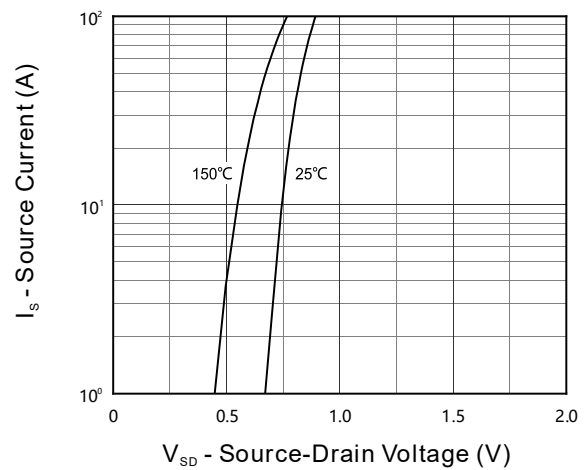


Figure 10. Diode Forward Current

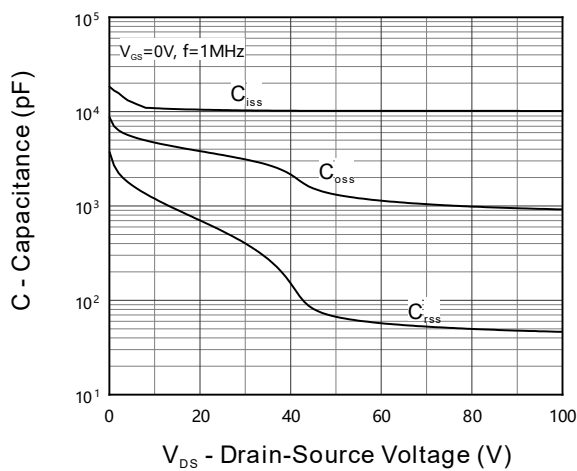


Figure 11. Capacitance

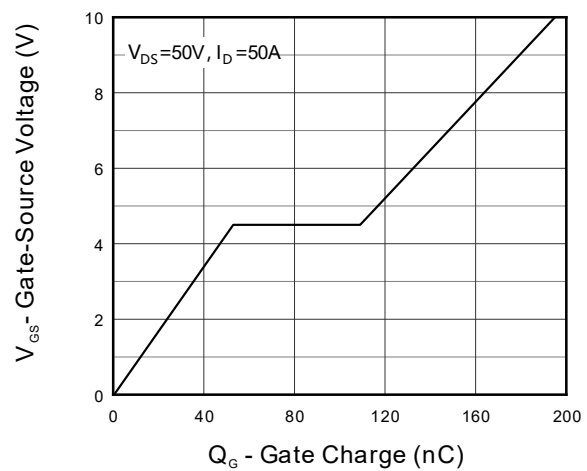
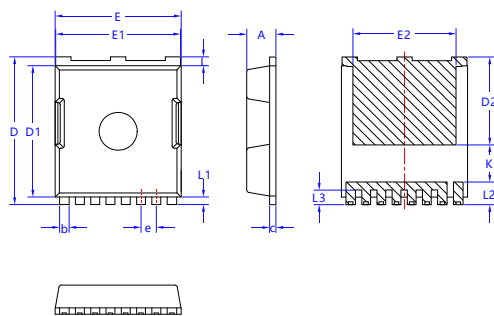
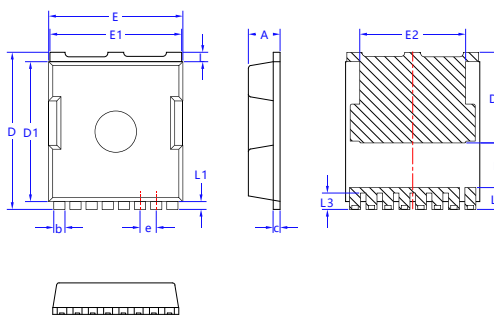


Figure 12. Gate Charge

8. Package Dimensions

TOLL-8L Package

Outline A / 外形A					Outline B / 外形B				
									
Symbol	Dimensions in Millimeters				Symbol	Dimensions in Millimeters			
	MIN	NOM	MAX			MIN	NOM	MAX	
A	2.20	2.30	2.40		A	2.20	2.30	2.40	
b	0.60	0.70	0.90		b	0.70	0.80	0.90	
c	0.40	0.50	0.60		c	0.40	0.50	0.60	
D	11.48	11.68	11.88		D	11.48	11.68	11.88	
D1	10.28	10.38	10.55		D1	10.28	10.38	10.55	
D2	6.85	6.95	7.05		D2	6.50	6.70	6.90	
E	9.80	9.90	10.0		E	9.80	9.90	10.0	
E1	9.70	9.80	9.90		E1	9.70	9.80	9.90	
E2	8.00	8.10	8.20		E2	7.60	7.80	8.0	
e	1.20 BSC				e	1.20 BSC			
L	0.60 TYPE				L	0.60 TYPE			
L1	0.60 TYPE				L1	0.60 TYPE			
L2	1.60	1.80	2.10		L2	1.60	1.90	2.10	
L3	1.00	1.15	1.30		L3	1.00	1.15	1.30	
K	2.90 TYPE				K	4.18 TYPE			

Note: As a single packaging production line cannot meet market demands, this product will be independently produced on two production lines. The outlines on different production lines may vary slightly, and the two outlines will be randomly shipped.

说明：由于单一封装产线难以满足需求，本型号需在两条产线进行生产，不同产线封装外形略有差异，两种外形随机出货。