

Dual N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☒ Surface-mounted package
- ☒ ESD:2KV
- ☒ Advanced trench cell design

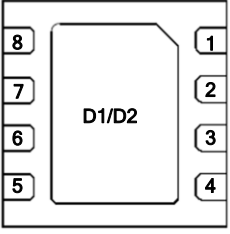
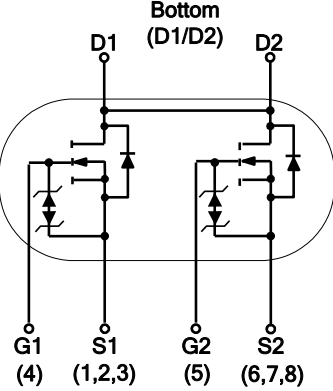
1.2 Applications

- ☒ Motor application
- ☒ High power inverter system

1.3 Quick reference

- ☒ $BV \geq 18V$
- ☒ $P_{tot} \leq 31W$
- ☒ $I_D \leq 50A$
- ☒ $R_{DS(ON)} \leq 5.6m\Omega @ V_{GS} = 4.5V$
- ☒ $R_{DS(ON)} \leq 7.8m\Omega @ V_{GS} = 2.5V$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1,2,3	Source(S1)		
4	Gate(G1)		
5	Gate(G2)		
6,7,8	Source(S2)		
		Bottom View DFN3x3-8L	

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_C=25^{\circ}C$	18	-	V
V_{GS}	Gate-Source Voltage	$T_C=25^{\circ}C$	-	± 12	V
$I_{D^{*,***}}$	Drain Current	$T_C=25^{\circ}C, V_{GS}=10V$	-	50	A
		$T_C=100^{\circ}C, V_{GS}=10V$	-	34	A
$I_{DM^{*,***}}$	Pulsed Drain Current	$T_C=25^{\circ}C, V_{GS}=10V$	-	68	A
P_{tot}	Total Power Dissipation	$T_C=25^{\circ}C$	-	31	W
T_{stg}	Storage Temperature		-55	150	$^{\circ}C$
T_J	Junction Temperature		-55	150	$^{\circ}C$
I_S	Diode Forward Current	$T_C=25^{\circ}C$	-	34	A
$R_{\theta JC^{*}}$	Thermal Resistance-Junction to Case		-	4	$^{\circ}C/W$

Notes:

- * Surface Mounted on 1 in² pad area, $t \leq 10$ sec
- ** Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- *** Limited by bonding wire

4. Marking Information

Product Name	Marking
KJ3350Q	3350Q YWWXXX YWWXXX: Date Code

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ3350Q	DFN3x3-8L	6'		3000	
		13'		5000	

Note: KUAJIEXIN defines "Green" as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C)

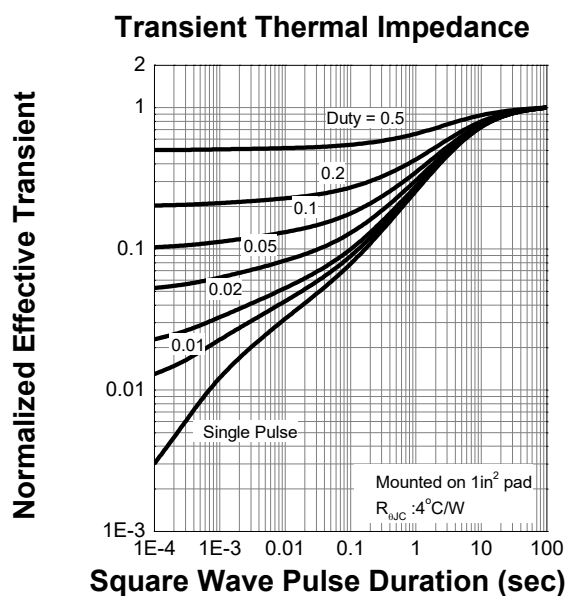
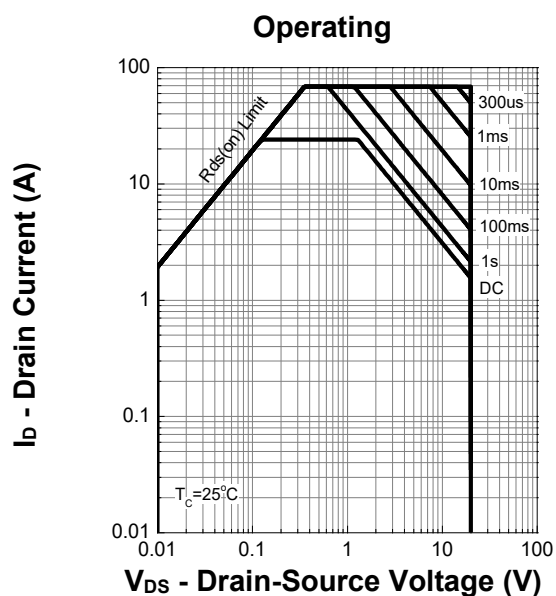
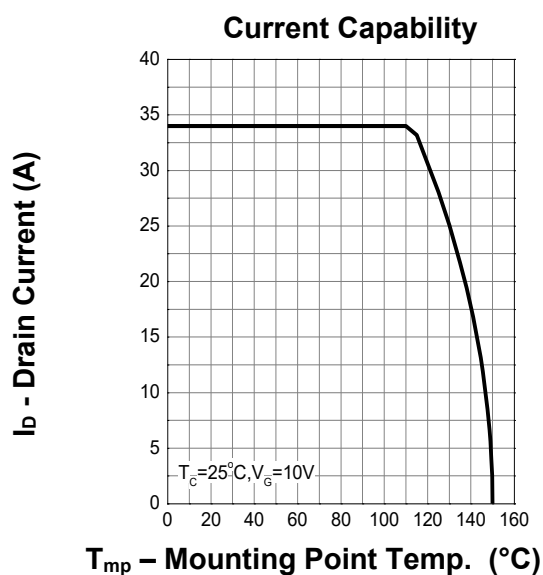
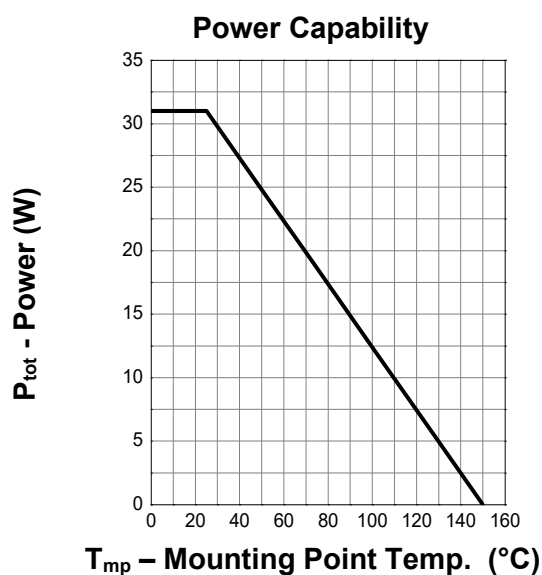
6. Electrical Characteristics (T_A=25°C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	18	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	0.5	-	1.0	V
I _{DSS}	Drain Leakage Current	V _{DS} =18V, V _{GS} =0V	-	-	1	μA
		T _J =85°C	-	-	30	μA
I _{GSS}	Gate Leakage Current	V _{GS} =±10V, V _{DS} =0V	-	-	±10	μA
R _{DS(ON)} ^a	On-State Resistance	V _{GS} =4.5V, I _{DS} =20A	-	5	5.6	mΩ
		V _{GS} =2.5V, I _{DS} =10A	-	6	7.8	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} =20A, V _{GS} =0V	-	-	1.2	V
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =10V Frequency=10KHz	-	2017	-	pF
C _{oss}	Output Capacitance		-	278	-	
C _{rss}	Reverse Transfer Capacitance		-	259	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} =10V, V _{GEN} =10V, R _G =4.5Ω, R _L =0.5Ω, I _{DS} =20A	-	0.3	-	μs
t _r	Turn-on Rise Time		-	0.75	-	
t _{d(off)}	Turn-off Delay Time		-	6.2	-	
t _f	Turn-off Fall Time		-	3.7	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =10V, I _{DS} =20A	-	34.6	-	nC
Q _{gs}	Gate-Source Charge		-	6.4	-	
Q _{gd}	Gate-Drain Charge		-	8.8	-	

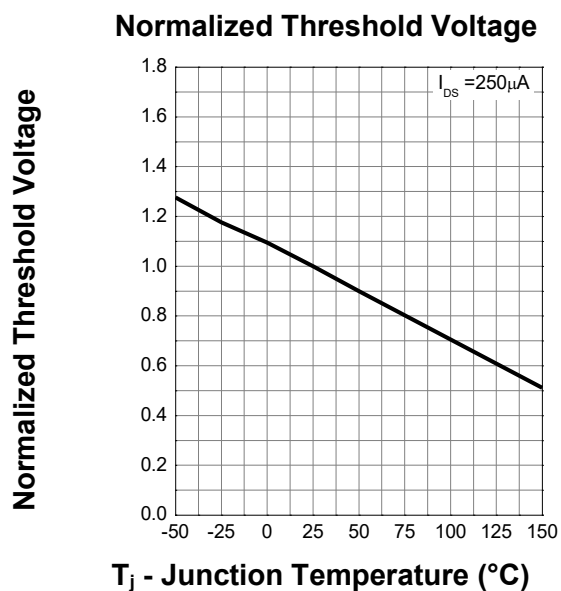
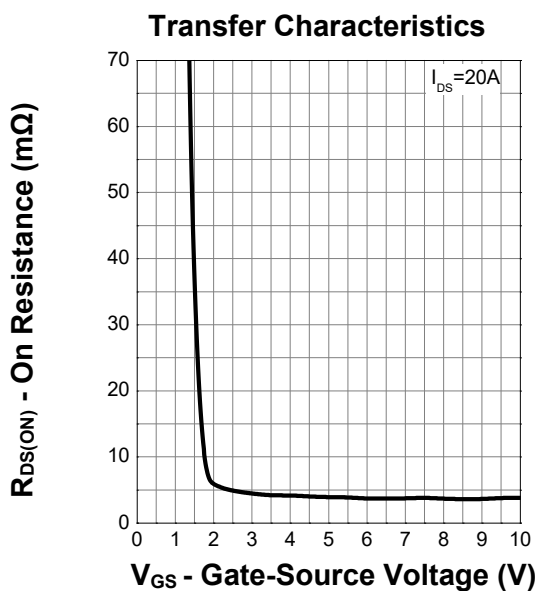
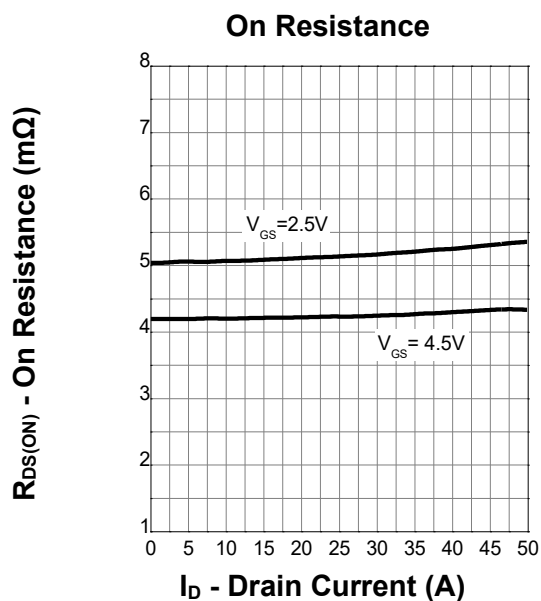
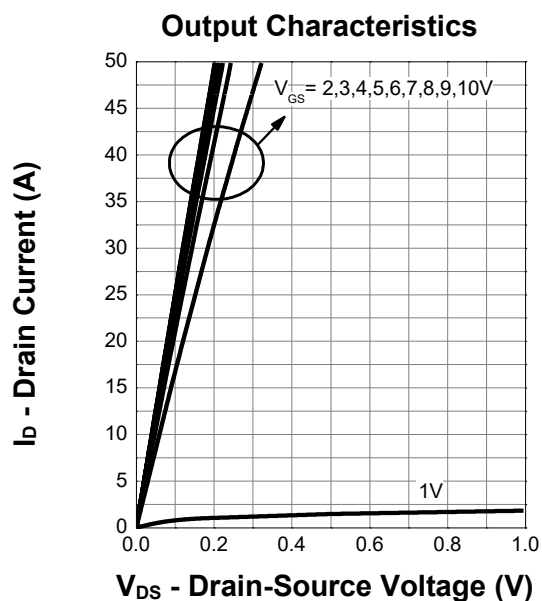
Notes:

- a. Pulse test; pulse width ≤ 300μs, duty cycle ≤ 2%
- b. Guaranteed by design, not subject to production testing

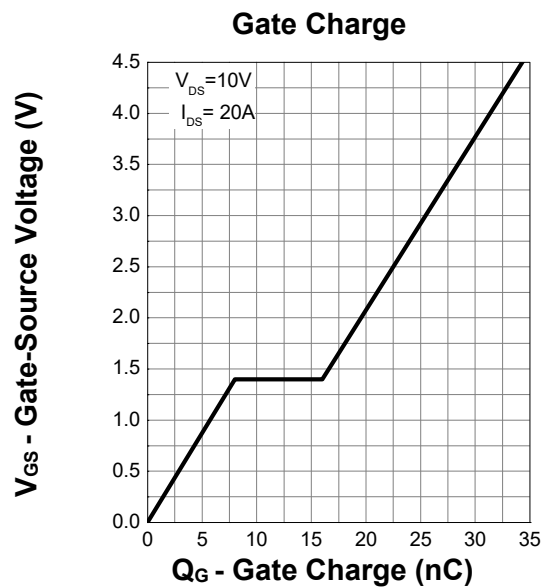
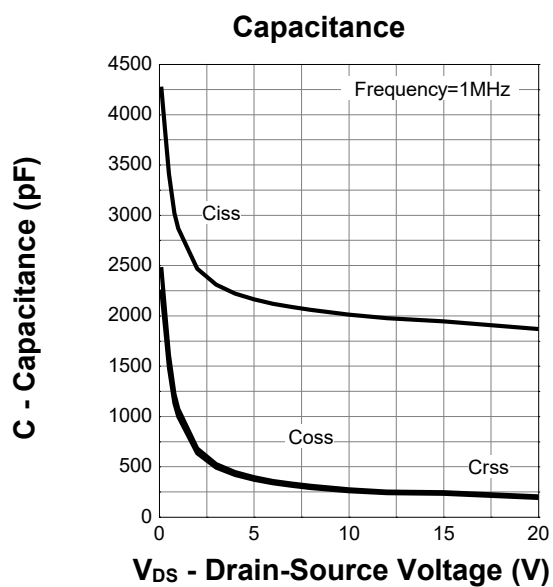
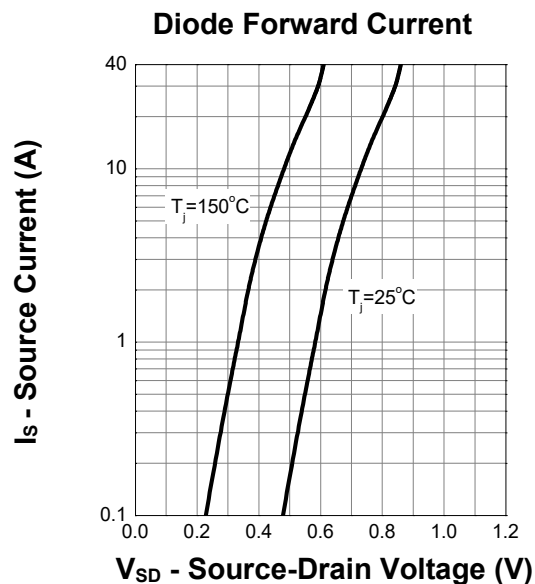
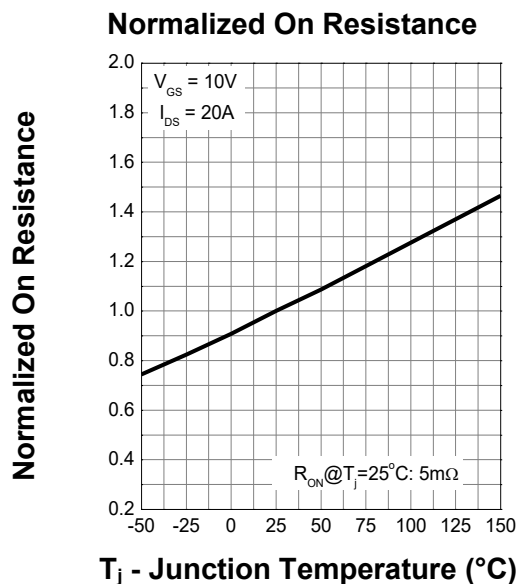
7. Typical Characteristics



7. Typical Characteristics (cont.)



7. Typical Characteristics (cont.)



8. Package Dimensions

DFN3x3-8L Package

